A Test-driven Methodology for Real-time On-line Temperature Prediction and Power Estimation

Jaeha Kung, Minki Cho, Sudhakar Yalamanchili, and Saibal Mukhopadhyay
School of ECE, Georgia Institute of Technology, Atlanta, GA 30332, USA

***Abstract* – A methodology is developed for fast, on-line, and real-time estimation of transient variations in temperature and average power of an IC after fabrication and packaging and experimentally demonstrated in a 130nm CMOS test-chip.**

I. INTRODUCTION

Due to the increased integration density and operating frequency, the dynamic and leakage power of ICs has increased significantly with scaling [1]. A higher power density results in elevated chip temperature which further increases the leakage current (leakage-temperature feedback). High temperature during test or operation degrades circuit reliability. Temperature can be more challenging to control during test than regular operation as the test-power can be much (3X to 30X) higher [2-3]. Hence, power and thermal aware test scheduling to minimize test time while satisfying maximum power or temperature constraint has emerged as a critical research area [4-6].

Fast, accurate, real-time and on-line estimation of transient temperature is crucial for efficient power/thermal management during test or operation. The detail thermal simulation tools like Hotspot are often used to estimate temperature to support power/thermal-aware test scheduling [7-9]. These simulators are accurate but require appreciable computation time to estimate temperature. Moreover, they do not capture the effect of post-silicon variations in thermal properties or leakage which can result in different temperature for same dynamic power [10-13]. Therefore, detail thermal simulators, although very useful for design time thermal analysis, are less suitable for real-time and on-line temperature prediction.

Likewise real-time on-line sensing and characterization of transient variations in average power dissipation is also challenging. The design time average power estimation tools are significantly slow for use in real-time. The dynamic variation of instantaneous power can be monitored using on-line current sensors [14] or by sensing voltage variation across a sleep transistor [15]. Designing current or power sensors are challenging at low operating voltages. Moreover, when an average or a slowly varying power pattern is needed, the above approaches will require additional filtering circuits or incur significant memory overhead.

This paper presents a methodology for fast, on-line, and real-time estimation of transient variations in temperature and average power of individual ICs after fabrication/packaging. The proposed method exploits the relation between power dissipation and temperature. The proposed approach is based on the post-silicon thermal analysis methodology, Thermal

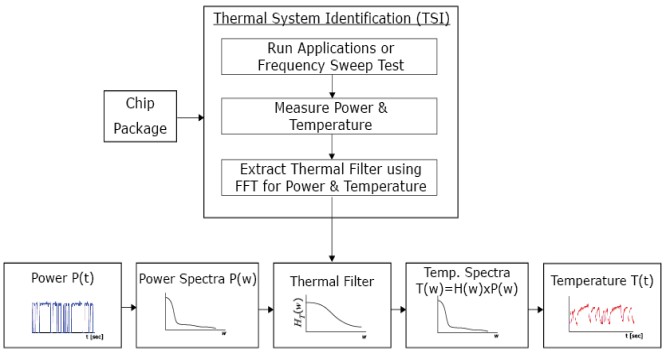

Figure 1. The basic concept of *Thermal System Identification* (TSI) method [12].

System Identification (TSI), presented by Cho et. al. [12] (Fig. 1). TSI characterizes the thermal system of an IC in frequency domain by power and thermal measurement (thermal filter). Next, the thermal filter is used to estimate temperature for a given power pattern using transformation between time and frequency domain. The fundamental theory of TSI is presented in [12] and verified experimentally in [13]. This paper utilizes TSI to design time domain filters for efficient on-line and real-time temperature and power estimations. The time-domain filters eliminate the need to compute complex Fourier and Inverse Fourier Transform required in the previous TSI based approaches [12]. The paper makes the following contributions:

- An on-chip time-domain thermal filter is proposed to represent the thermal system. The filter is tuned post-silicon to represent the frequency response of the thermal system an IC extracted by TSI.
- The extracted thermal filter transforms given power to predicted temperature. An inverse filter is designed based on the extracted filter to capture the inverse relation and estimate power from a measured temperature pattern.
- An overall characterization flow is presented that generates unique time-domain filters for each IC using TSI for on-line real-time power and thermal estimation.

The proposed time-domain temperature and power estimation method is experimentally validated through a 130nm CMOS test-chip using on-chip heaters and temperature sensors [13]. The proposed time-domain filter can enable on-line power and temperature prediction facilitating power/thermal aware test.

The rest of the paper is organized as follows: Section II presents the background on the TSI method; Section III and IV describes the forward and inverse time-domain thermal filters, respectively; Section V presents the test flow; Section VI presents the measurement results; and Section VII summarizes the paper.

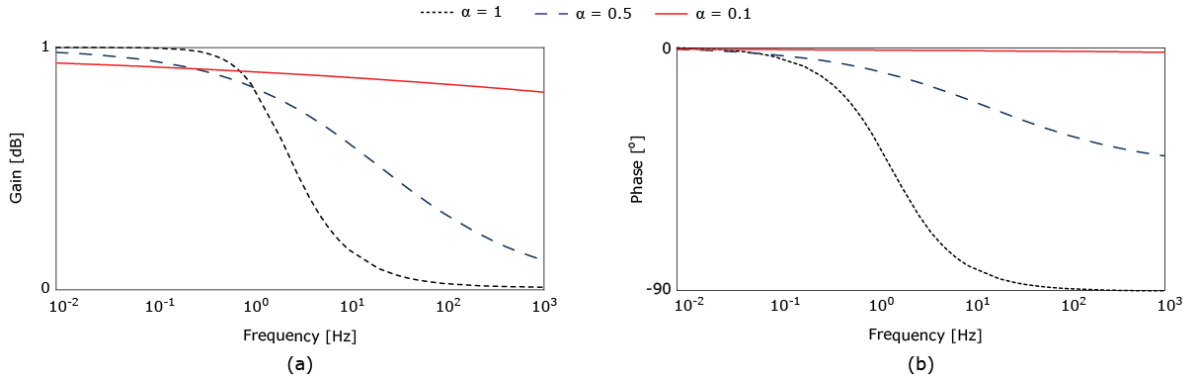

Figure 2. Frequency response of FLPF: (a) magnitude response, (b) phase response with different α value (0.1, 0.5, and 1).

II. Background: Thermal System Identification

Most thermal analysis methods require accurate characterization of the basic thermal properties such as heat capacity and thermal conductivity to determine temperature for a given power pattern [7-9]. Extraction of such properties requires complex measurements and characterizations [16]. Moreover, these properties can have chip-to-chip or time-dependent variations; for example, the properties of thermal interface material (TIM) can vary due to effects like delamination. Finally, due to the positive feedback between leakage and temperature, the chip-to-chip variation in process (hence, leakage) can result in chip-to-chip variation in temperature for same power pattern. A post-silicon thermal analysis methodology - *Thermal System Identification (TSI)*- has been proposed to deal with inherent variations after fabrication of the chip [12]. In TSI, a frequency response of a thermal system is extracted post fabrication and packaging through power and thermal measurements to capture the variations in the thermal characteristics of a particular IC.

TSI exploits the well-known analogy between electrical and thermal system. By this analogy, temperature is analogous to voltage, heat is analogous to current, thermal conductivity is analogous to resistance (R), and heat capacity is matched to capacitance (C). This analogy forms the basis of thermal analysis using distributed RC network [7]. The first-order RC circuit is a simple low-pass filter which makes it possible to think of a thermal system as a complex low-pass filter. Also, RC network is a linear system which enables application of superposition principle [12].

For a simple understanding of TSI, assume a single point (x, y) on a given chip. Power consumption, $P(t)$, at location (x, y) is also assumed to be given. Temperature, $T(t)$, is then obtained by performing a convolution between power and the impulse response of thermal system, $h_T(t)$. It can be written as

$$T(t) = P(t) * h_T(t). \quad (1)$$

The convolution operation is simply a multiplication in frequency domain. Then, Fourier Transform of (1) becomes

$$T(w) = P(w) \times H_T(w), \quad (2)$$

where $H_T(w)$ is the frequency response of a thermal system

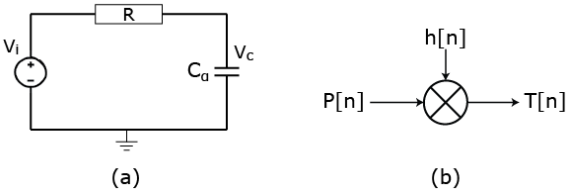

Figure 3. (a) Simple RC_α circuit and (b) a block diagram of the digital system for the time domain filter design.

between the power generation and temperature observation point. Thus, we can define *Thermal System Identification* as a method to identify $H_T(w)$ by the relation of (2). TSI exploits the presence of on-chip temperature sensors at various locations of a chip. Essentially one can apply a periodic power pattern with varying frequency and estimate the associated temperature variation from the sensors at different locations. The measured result can be used to construct the amplitude and phase response of the thermal filters between the locations of power dissipation to the locations of temperature sensors. The overall flow of TSI is shown in Fig. 1. TSI method can be included in a test flow to extract $H_T(w)$. In the following sections we present forward or inverse thermal filter using the extracted $H_T(w)$ to obtain real-time estimates of temperature or power variations of the chip, respectively.

III. Design of Time-Domain Forward Thermal Filter to Estimate Temperatur Variation

The thermal filter extracted by the TSI method can be used to predict transient temperature for a given power pattern. As demonstrated by Cho et. al, this can be performed by first performing Fourier Transform on the power pattern ($P(w)$); next multiplying $P(w)$ with the thermal filter ($H_T(w)$) to obtain the frequency response of temperature ($T(w)=P(w)\cdot H_T(w)$; and finally, performing Inverse Fourier Transform on $T(w)$ to estimate the transient temperature pattern. While the above approach enables post-silicon temperature prediction, it incurs the complexity associated with transformations between time and frequency domain. If we design a low pass filter having a similar behavior as the extracted thermal filter $H_T(w)$, it is possible to directly predict the time domain variations in temperature from the time domain power pattern without the need for complex Fourier and Inverse Fourier Transform. The

problem becomes how to implement an on-chip low pass filter having same frequency response as the extracted thermal filter.

Temperature changes slowly which implies a large time constant. In other words, thermal filter has a quite low cutoff frequency. It is difficult to implement such a large time constant due to several design limitations, such as practical capacitor size, low noise level, and available dynamic range [17]. Circuits using switched-capacitor or G_m-C techniques were proposed to implement low cut-off frequency filters [18, 19]. However, the gain of the thermal filter response may decrease slowly, having a slope less than -20dB/decade, which will be noticed in Section VI. Low cut-off frequency filters are not only complex circuits, but also have a sharper transition having multiples of -20dB/decade. Therefore, we first explore a purely mathematical realization of the thermal filter having a flexible slope in gain and phase response. It is difficult to satisfy a smoothly decreasing frequency response by simply controlling poles and zeros. However, there is a methodology making it possible; a low pass filter using a fractional order capacitor [20]. Conceptually, a fractional order capacitor (FOC) is an element whose current and voltage are related by

$$i(t) = \frac{Cd^{\alpha}v(t)}{dt^{\alpha}}. \tag{3}$$

The forward thermal filter response can be designed by a fractional order low pass filter (FLPF) having a transfer function as follows:

$$H_{FLPF}(s) = \frac{A_{DC}}{s^{\alpha} + w_f}, \tag{4}$$

where w_f is a fractional cutoff frequency (= 1/RC), α is an exponent coefficient, and A_{DC} is a DC gain control variable. Then, the magnitude and phase response of a designed filter, equivalently FLPF, will become

$$Gain = |H(jw)| = \frac{A_{DC}}{\sqrt{w^{2\alpha} + 2\alpha w^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right) + w_f^2}},$$
$$Phase(\text{rad}) = \angle H(jw) = -\tan^{-1}\frac{w^{\alpha}\sin\left(\frac{\alpha\pi}{2}\right)}{w^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right) + w_f}. \tag{5}$$

When α = 1, (4) becomes a conventional first-order low pass filter amplified by A_{DC}/w_f. By controlling α, magnitude and phase response can be adjusted to fit an extracted thermal filter response from TSI method. The magnitude and phase response with different α value is shown in Fig. 2 (w_f is set to 20π rad). The frequency response of the filter is written as

$$\widehat{H}(jw) = |H(jw)| \cdot \angle H(jw). \tag{6}$$

Realization of a FOC is being studied for a decade [21, 22]. Electrolytic process is widely studied to develop FOC with target specifications such as its impedance [21]. It is realized when the probe with porous film on its electrodes is dipped into a polarizable medium; the property of porous film decides characteristics of the designed FOC. Also, a FOC has been realized by developing fractal structures on MOS layers [22]. Certain fractal structures on metal layer provide fractional order properties (3). Even though such processes are yet commercialized in industry, they show possibility of a hardware device satisfying (4). Using an actual FOC, the thermal filter can be designed by a simple RC_{α} circuit (Fig. 3(a)).

As mentioned above, the FOC is not yet a commercial device. Therefore, we present a functional filter that can be implemented using digital system (Fig. 3(b)). Performing inverse Laplace Transform on (4) when α = 0.5 gives a time-domain impulse response $h(t)$, which is

$$h(t) = A_{DC}\left[\frac{1}{\sqrt{\pi t}} - w_f \cdot e^{w_f^2 t}\cdot erfc\left(w_f\sqrt{t}\right)\right], \tag{7}$$

where erfc(·) is the complementary error function. In time domain temperature prediction, the convolution operation is required to predict temperature with a given power pattern. Assume $h[n\cdot T_s]$ is stored in a lookup table (LUT) to increase the speed of computation. To understand the computational efficiency of the time-domain filtering, consider temperature prediction for one second with a given power pattern sampled at T_s = 1ms (the number of sample n is 1,000). The convolution requires n^2 of multiplication. If the multiplication is performed with 1GHz clock frequency, temperature is predicted in 1ms with a very simple circuit (only a multiplier required). In other words, given the expected power pattern, a temperature evolution of 1 second can be predicted within ~1ms. It shows the feasibility of the real-time temperature prediction.

IV. Design of Time-Domain Inverse Thermal Filter to Estimate Power Variation

The on-line sensing and characterization of average power dissipation can significantly facilitate both test and operation. In this section, we present a methodology to characterize power variation over a finite duration from the measured temperature and using inverse thermal filter. During the power pattern characterization, a thermal filter response is assumed to be extracted using TSI. Similar to a time-domain thermal filter, an inverse thermal filter can be designed to characterize power from the measured temperature. From (2), we obtain:

$$P(w) = T(w) \times H_T^{-1}(w). \tag{8}$$

The problem becomes how to implement a filter circuit which behaves similarly as $H_T^{-1}(w)$. For given location (x,y), $H_T^{-1}(w)$ simply becomes $1/H_T(w)$; dividing (2) by $H_T(w)$ has to be equal to (8). For the inverse thermal filter, the slope as well as the cutoff frequency also has to be controlled in detail to satisfy any extracted thermal filter. In this case, inverse thermal filter response can be designed by modifying (5), which becomes:

$$\text{Gain} = |H^{-1}(jw)| = \frac{\sqrt{w^{2\alpha} + 2\alpha w^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right) + w_f^2}}{A_{DC}} \tag{9a}$$

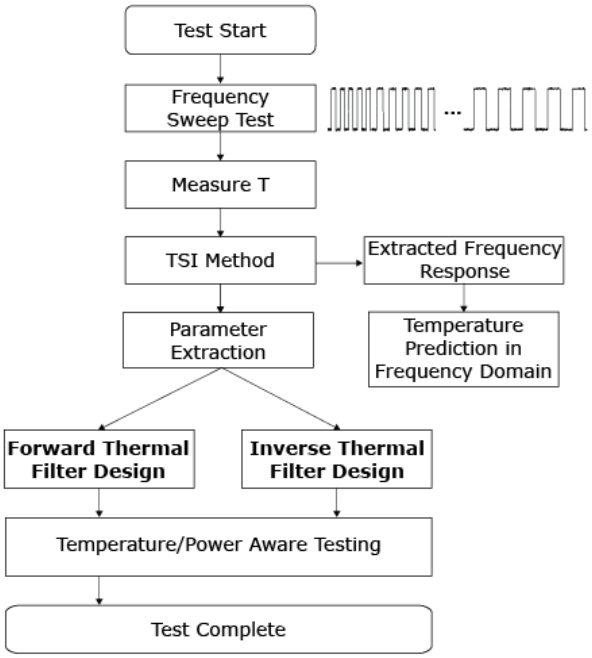

Figure 4. Test flow including time domain thermal filter design.

$$Phase\ (°) = \angle H(jw) = \tan^{-1}\frac{w^{\alpha}\sin\left(\frac{\alpha\pi}{2}\right)}{w^{\alpha}\cos\left(\frac{\alpha\pi}{2}\right) + w_f}, \quad (9b)$$

where A_{DC} is DC gain control variable, w_f is a fractional cutoff frequency, and α is an exponent coefficient. Similar to forward filter case, the time domain impulse response, $h^{-1}(t)$, can be obtained by the inverse Fourier Transform of $H_T^{-1}(w)$. It is merely a mathematical derivation as in Section III. Although the frequency response of inverse thermal filter is similar to a high pass filter, high frequency components of power could not be completely restored due to low pass filtering effect of temperature. Thus, power characterization with the inverse thermal filter will be useful when estimating average or slowly varying power pattern.

V. Test Flow

TSI method can be included in a test flow to extract $H_T(w)$. Using extracted $H_T(w)$, forward or inverse thermal filter can be designed providing the real-time feedback on temperature or power of the chip. The test flow using time domain thermal filter is shown in Fig. 4. After the chip is fabricated, the periodic test patterns are applied generating period voltage variations with varying fundamental frequency. We refer to this as the *frequency sweep test*. The test can be performed by running a given test vector in the core for a time-interval T/2 which defines the 'high' period of the power pulse. The core (or IC) is taken to a low power (idle) mode for the next T/2 period. One way to create such a period power pattern is to exploit power gating (or core gating) as discussed in [12]. Temperature is then measured from the thermal sensor for each input frequency of the power pulse. Fourier Transform is performed on each power and temperature to obtain the specific frequency response of the chip under certain variations; H(w) is obtained by dividing T(w) by P(w).

Based on the extracted thermal filter, time-domain forward or inverse thermal filter is designed by deciding parameters in (5) or (9) to match the extracted thermal filter. When thermal-aware test is performed, time-domain forward thermal filter is used to estimate temperature in real-time. Power pattern is assumed to be given in this case; power consumption of predetermined test vectors is known. For power-aware testing, time-domain inverse thermal filter is used to estimate slowly varying power pattern in real-time. In this testing mode, temperature measured from the thermal sensor is used to accurately estimate a test power pattern of the circuit.

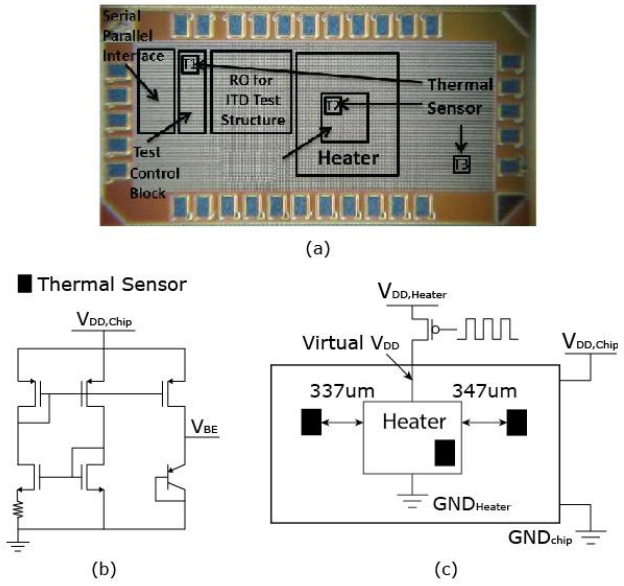

Figure 5. Test structure for TSI verification: (a) a die photo of the test chip, (b) a BJT-based thermal sensor, and (c) a schematic of test circuit.

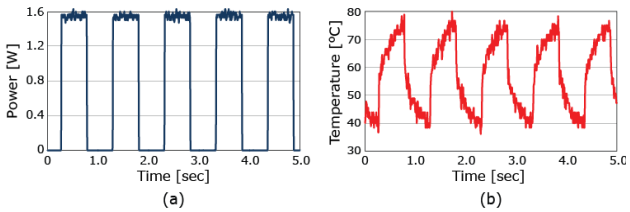

Figure 6. AC analysis for thermal filter response extraction: (a) power profile by heater at 1 Hz and (b) temperature obtained by thermal sensor.

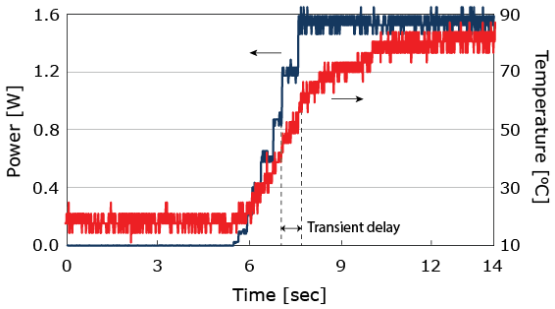

Figure 7. Transient response of temperature (red) right after input power (blue) is applied during the DC analysis.

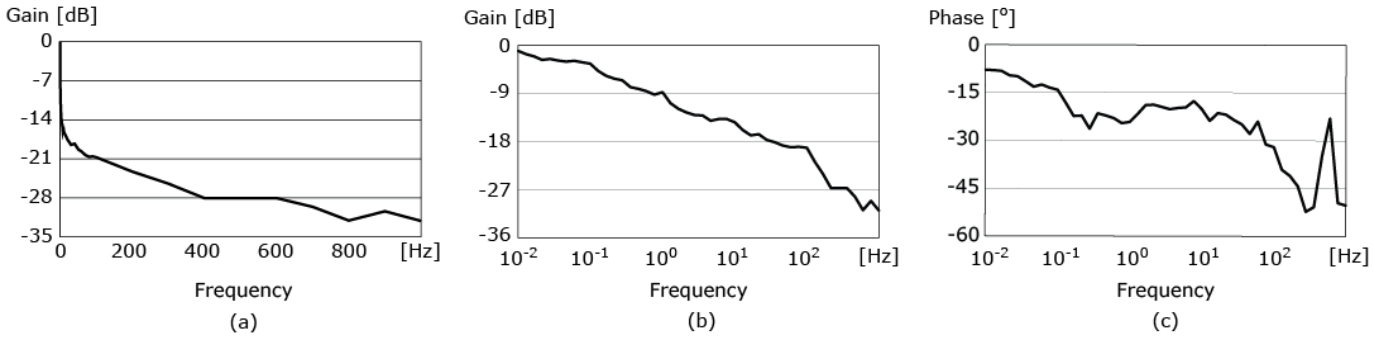

Figure 8. Extracted thermal filter response by TSI method: (a) the amplitude response in linear scale, (b) in logarithmic scale, and (c) the phase response in logarithmic scale.

VI. Experimental Results

A. Test Chip and Experimental Setup

For the verification of TSI method described in Section II, a test chip (2 mm^2) has been designed (Fig. 5(a)) [13]. The package used for the test chip is Leadless Chip Carrier (LCC) package using 44 pins. $V_{DD,Chip}$ is allowed from 0.55V to 1.2V. Three analog BJT-based thermal sensors are placed near a heater to measure temperature. A simple structure of a test system is shown in Fig. 5(c). There are three important components; a poly-based heater, an external PMOS, and a thermal sensor. To heat up the test chip, a poly-based heater is placed inside the chip. Power density of the chip is estimated by dividing the dissipated total power of the heater (= $V^2_{DD,heater}/R$) by the chip area. Since resistance R of the heater is fixed to 40Ω, power can be estimated by controlling $V_{DD,heater}$ from 0V to 10V. An external PMOS is used to control this $V_{DD,heater}$. Thus, the gate of PMOS is connected to a function generator providing a square wave (equivalently, a power pattern) with different frequencies. Increasing a fundamental frequency enables us to perform AC analysis of the thermal system as described in the next subsection.

A BJT-based analog thermal sensor is used as shown in Fig. 5(b). The output voltage, V_{BE}, of the thermal sensor is negatively proportional to actual temperature. Temperature rise affects several factors which increase the current of a BJT; saturation current I_S, beta β, and mobility μ. To compensate such current increase to maintain it constant, V_{BE} is reduced accordingly. An experiment is done to directly show the temperature-V_{BE} dependency using our thermal sensor. Initial V_{BE} at ambient temperature ($T_{ambient}$ is set to 20℃) is used as a reference, which was 776mV. Then, $V_{DD,heater}$ is increased from 1V to 7V. Temperature of the chip is found based on a simulated V_{BE}. As a result, V_{BE} is reduced by ~107mV for ~1W increase of a heater power; corresponds to increase of a simulated temperature by ~60℃. Thus, the V_{BE}-temperature dependence can be formulated as:

$$\mathrm{T} = \frac{V_{BE,ambient} - V_{BE,sensor}}{0.0018} + T_{ambient}. \quad (10)$$

The temperature is calculated by transforming the output voltage of a thermal sensor by (10) throughout our experiment.

B. Thermal Filter Response Extraction

Using the test chip discussed in Section VI.A, the magnitude and the phase response of a thermal system can be extracted at a given frequency [12-13]. The frequency response of the thermal system obtained by TSI method is referred to as a *thermal filter response* throughout this paper. Fundamental frequencies from 0Hz to 1kHz (47 data points) are used to extract the thermal filter response.

1) *AC Analysis*: During an AC analysis, a square wave with a fixed fundamental frequency is applied at the gate of external PMOS of test circuit. It controls the virtual V_{DD} of the heater inside the chip so that the power pattern becomes as shown in Fig. 6(a). As mentioned in Section II, thermal system is expected to show a response similar to a low-pass filter; the temperature changes slowly with respect to the power transition. Frequencies from 0.01Hz to 1kHz, increased in a logarithmic scale, are tested. In Fig. 6, a periodic power pattern with 1Hz frequency and its resulting temperature are depicted. There is some delay for temperature to follow the change of instantaneous power which can be interpreted by the phase response. By performing Fourier Transform for both power and temperature, the magnitude and phase information of thermal filter response at 1 Hz can be obtained by relation (2). Similar experiments are done at other frequencies to obtain the amplitude and the phase response of the thermal filter at all frequencies.

2) *DC Analysis*: For a DC analysis, 0V is applied to the gate of an external PMOS so that to provide ($V_{DD,heater}$–V_{th}) to the heater. To get an accurate DC gain, voltage is applied for five minutes. After the steady state is reached, DC gain is achievable by dividing temperature ($T - T_{ambient}$) by the heater power. DC gain of our thermal system was about 45. Although there is no phase response in DC case, an initial transient response occurs as shown in Fig. 7. In the experiment, the transient delay marked in Fig. 7 was about 1.2 seconds. This is accounted for using an empirical decaying function:

$$f_{decay}(t) = 1 - \exp\left(-\frac{t}{\tau}\right) \quad (11)$$

where τ is a time constant to control decay rate; it becomes 63.2% of maximum value at τ. Based on our *DC analysis*, τ is set to 2.4 seconds.

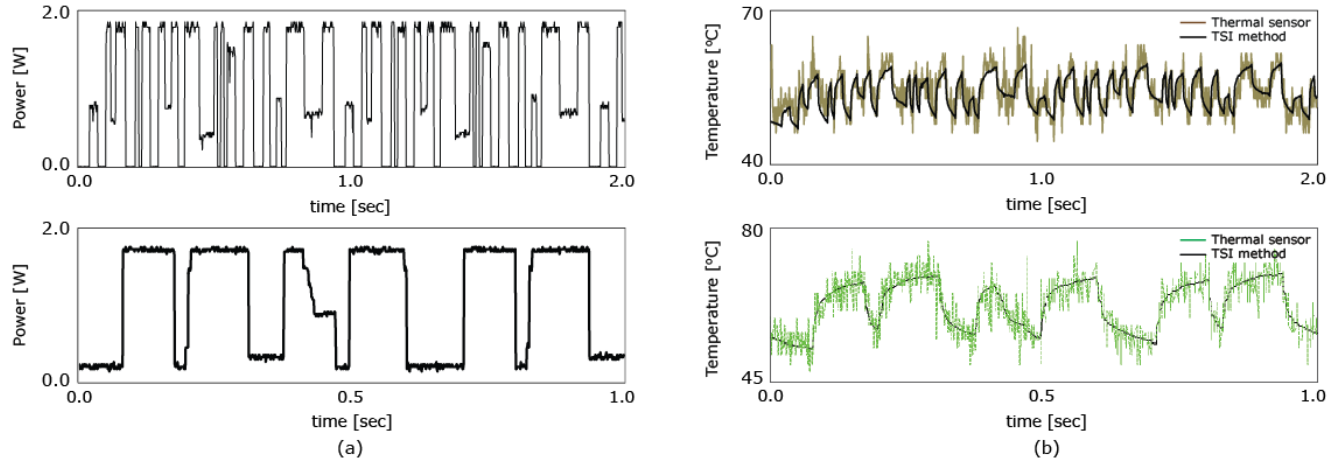

Figure 9. TSI method verification: (a) input power patterns, (b) comparison of temperature obtained from a thermal sensor (color) and the TSI method (black) for each power pattern.

After both AC and DC analyses, a post-silicon thermal filter can be extracted with considering any variations reside in the chip. As shown in Fig. 8, it shows the filter response like a low-pass filter as expected in Section II. As shown in Fig. 8(a), the gain sharply decreases at very low frequencies. This simply becomes a smoothly decreasing curve in logarithmic scale as in Fig. 8(b), which is about -6dB/ decade. Note that the 3dB point is at ~0.1Hz which is a very low frequency. Also, the phase response of the thermal filter is shown in Fig. 8(c).

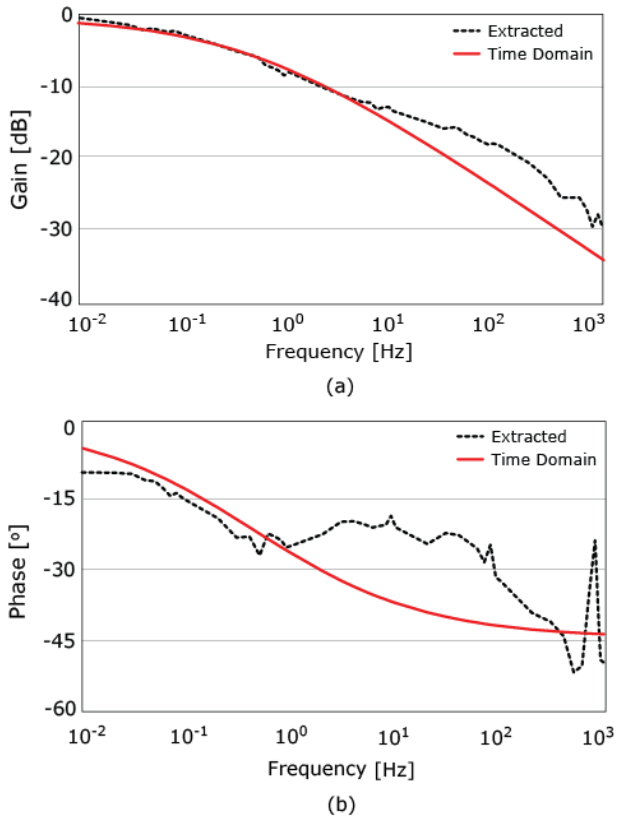

Figure 10. The time-domain thermal filter: (a) the amplitude response and (b) the phase response.

Although the accuracy of TSI has been verified in [12-13], we also study the same for completeness. The input voltage, to an external PMOS of the test structure, is generated by the National Instrument PXIe-6363 to generate power dissipation of the on-chip heater as shown in Fig. 9(a). For the test purpose, a multi-level and multi-frequency power patterns are provided. The figure shows 1,000 sampled data points which are determined by the number of stored data from the oscilloscope. Then, temperature for each power pattern is obtained by measuring V_{BE} of the thermal sensor; the sensor nearest to the heater is used for verification. It is converted into temperature by using (10). For the comparison, temperature is estimated by using the extracted thermal filter response and the Fourier and Inverse Fourier Transform method as shown in Fig. 1. Fig. 9(b) shows the accuracy in temperature measurement; colored line represents measured temperature from the thermal sensor while black solid line corresponds to estimated temperature by the TSI method. Considering that the very high-frequency fluctuations are mostly measurement noise, the extracted thermal filter can accurately estimate temperature.

C. Temperature Estimation with the Time-Domain Filter

As mentioned in Section III, time domain thermal filter is designed to predict temperature in real-time. To verify the method with the test chip, variables in (5) is set to match the extracted thermal filter. The half-power frequency, w_h, is used as a reference which satisfies:

$$\left|\hat{H}(\mathrm{j}w_h)\right| = \frac{1}{\sqrt{2}} \cdot \left|\hat{H}(jw_{passband})\right|. \tag{12}$$

Now, w_h can be obtained by:

$$w_h = w_f^{1/\alpha} \cdot \left(\sqrt{1 + cos^2\left(\frac{\alpha\pi}{2}\right)} - \cos\left(\frac{\alpha\pi}{2}\right)\right)^{1/\alpha}, \tag{13}$$

where α is set to 0.5 to fit the slope of the gain response, but also to simplify the inverse Laplace Transform for computing the time-domain impulse response $h(t)$ equals to (7). From the

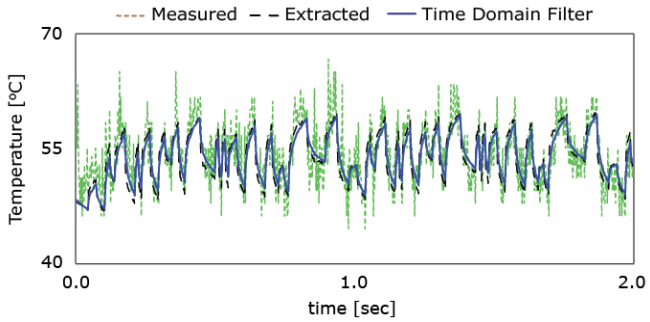

Figure 11. Temperature prediction result: measured temperature (green, dotted), the extracted thermal filter (black, dashed), and the time domain filter (blue, solid).

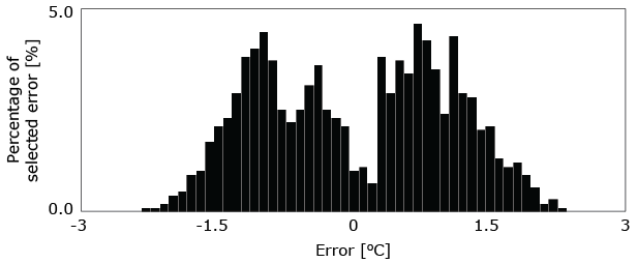

Figure 12. Histogram of error using the time domain thermal filter.

extracted thermal filter response, the gain reached half-power at ~0.13Hz. Using selected w_h and α, w_f is computed which is 0.7Hz. With these values for a time-domain thermal filter, frequency response of the designed time-domain filter is compared to the extracted thermal filter response which is shown in Fig. 10. Gain at lower frequencies is larger than higher frequencies. Thus, the accuracy both in the gain and the phase at lower frequency are more important than at higher frequency when selecting coefficients.

To show the accuracy of the time-domain thermal filter, the upper power pattern in Fig. 9(a) is used. From this power pattern, temperature is predicted with the extracted thermal filter plotted with a black dashed line in Fig. 11. The time-domain thermal filter is also used to predict temperature from the same power pattern. The result is compared to the

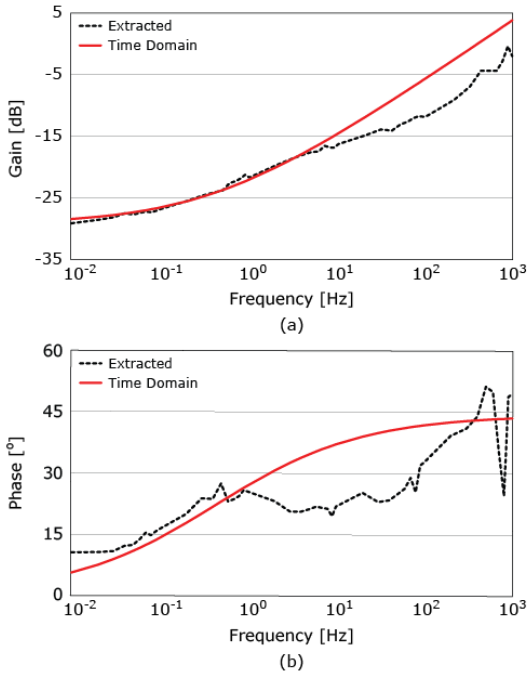

Figure 13. Comparison of inverse filter response between extracted thermal filter and time domain high pass filter: (a) the amplitude response and (b) the phase response in logarithmic scale.

temperature obtained by the extracted thermal filter as well as the measurement. As can be seen in Fig. 11, the temperature is predicted with high accuracy using proposed time-domain filter; plotted with a blue solid line. From Fig. 10, it is expected to have large error at which high frequency components exist; an abrupt power transition. Error is shown with a histogram where y-axis represents the percentage of selected error; total number of data is 1,000 (Fig. 12). The error is computed by ($T_{time\_domain} - T_{extracted}$). This error comes from either lower gain or phase at high frequency. However, the error is mostly within ±1.5℃ which is reasonable.

D. Power Estimation with the Time-Domain Inverse Filter

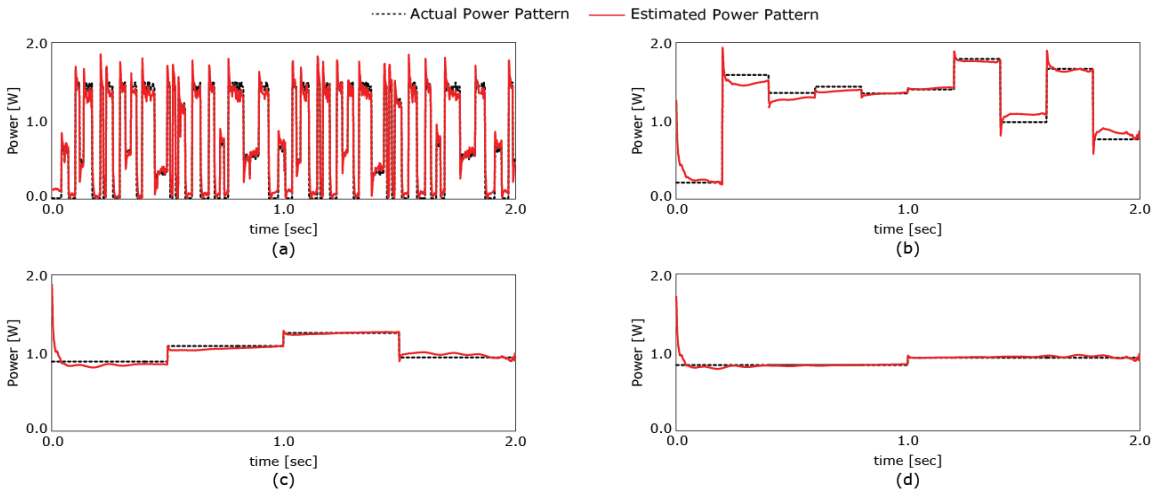

Figure 14. Power estimation using time-domain inverse thermal filter: (a) entire power pattern, (b) average power for each 0.2 seconds interval, (c) for each 0.5 seconds, and (d) for each 1 second.

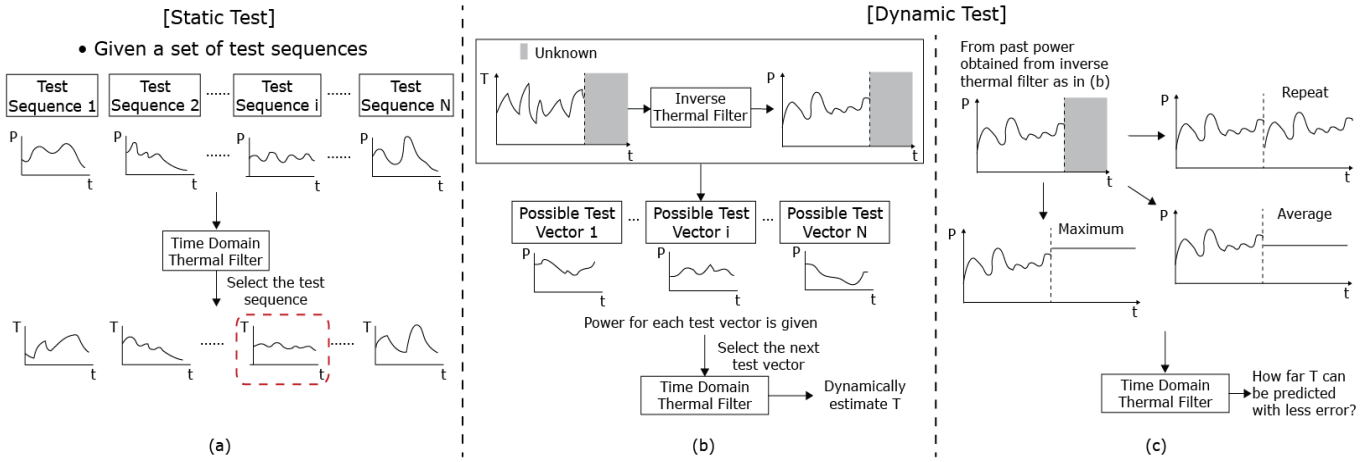

Figure 15. Applications of proposed time domain thermal filter: (a) static test for selecting test sequence and (b) dynamic test by selecting the next compatible test vector in real-time and (c) select future power pattern with less error when future power is unknown.

Assuming that the inverse filter response is extracted by the TSI method, an inverse thermal filter can be constructed. Fig. 13 shows the extracted inverse thermal filter (black line) and its time-domain approximation based on equation (9). The potential of the inverse thermal filter on power estimation is verified in Fig. 14. The power pattern with black dotted line (Fig. 14(a)) is used for verification. First, the power pattern with the black dotted line is applied to the test chip and the temperature sensor output is noted. The sensed temperature is filtered to eliminate the high-frequency noise (as observed in Fig. 9) and used as input to the time-domain inverse thermal filter. The output of the thermal filter is the estimated power which is shown as the red lines in Fig. 14. Comparison between actual power pattern and estimated one is evident from Fig. 14. As mentioned previously, high frequency data of the power pattern are lost by the nature of thermal behavior. Proposed time-domain inverse thermal filter is used to estimate power pattern. Due to larger gain at high frequencies (Fig. 13(a)), there are fluctuations at power transition points.

To stress the efficacy of characterizing a slowly varying power pattern, estimating average power for certain time interval is demonstrated. Three different time intervals are chosen for the experiment; 0.2, 0.5, and 1 second. As the time interval becomes larger, power estimation gets more accurate (less ripple within a time frame). Estimation error on average power over 2 seconds ranges from 0.22% (d) to 3.85% (a). Therefore, accuracy also increases in terms of estimating overall average power. Power estimation, using time-domain inverse thermal filter, with granularity of 0.5~1 second can be considered to be highly accurate.

E. Applications and Discussions

In the previous subsections we demonstrated the accuracy of the time-domain forward and inverse thermal filters. The real-time and on-line prediction of temperature can allow efficient thermal and power aware scheduling techniques. A direct application of the proposed filters is in static test (or task) scheduling where for each IC we can estimate the transient temperature for various possible scheduling options (Fig. 15(a)). However, a more interesting possibility is dynamic evaluation and prediction of the temperature pattern (Fig. 15(b-c)). As explained in the previous paragraph, the time-domain filters provide a computationally efficient method to estimate future temperature patterns for individual ICs for an expected power patterns. In other words, while scheduling a specific 'long' test (or task) pattern at any given time, it is possible to estimate the future temperature evolution using the proposed filter. However, the question is when only the current temperature and future power pattern is known, is it possible to obtain a reasonably accurate temperature prediction (Fig. 15(b))? As can be seen in a well-known heat conduction equation:

$$\rho C_p \frac{dT(x,y,t)}{dt} = \nabla[\kappa(x,y,t)\nabla T(x,y,t)] + g(x,y,t), \quad (14)$$

$dT(x,y,t)/dt$ can be calculated if entire power pattern is given or current temperature along with future power is known. The latter is the problem trying to solve here assuming that a thermal sensor is located at the point of interest. As the current temperature is known, predicting temperature requires dummy power pattern ahead of the given future power pattern to satisfy current temperature. As an example, consider a power pattern is unknown prior to 0.4 seconds of the power pattern shown in Fig. 9(a). In this experiment, transient delay will be considered as mentioned in (11). Then, temperature at 0.4 second is 25.6℃. The goal is to obtain this temperature with a small overhead; a short period of dummy power pattern. Assume 0.2 seconds of dummy power is applied to get 25.6℃. Thus, required average power P_{dummy} for 0.2 seconds to meet current temperature can be compute by:

$$(T_{curr} - T_{amb}) = A_{DC} \cdot P_{dummy} \cdot \left(1 - \exp\left(-\frac{t}{\tau}\right)\right), \quad (15)$$

where T_{curr} is the current temperature, T_{amb} is the ambient temperature, A_{DC} is the DC gain, and t = 0.2 sec. Then, P_{dummy} equals 1.9W from the given values. Fig. 16(a) shows efficacy of this approach by comparing predicted temperature with only future power and with entire power pattern. Note that the estimation accuracy can be improved even further by

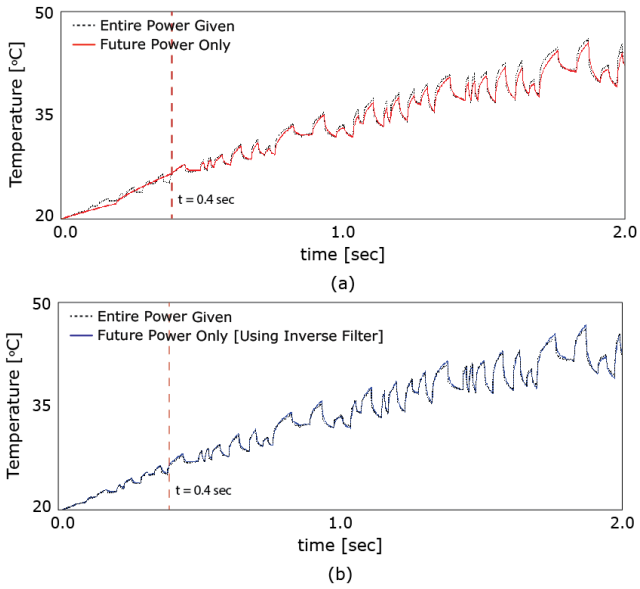

Figure 16. Temperature prediction with future power: (a) assuming P_{dummy} and (b) power pattern using the inverse thermal filter before time 't'.

computing the past power pattern using the inverse thermal filter (Fig. 16(b)).

An even more challenging problem arises when the future power pattern is not known. When there is only the past power pattern available, it is nearly impossible to accurately predict future temperature. However, an interesting question is how far future in the time temperature can be predicted within a given (say 0.5°C) error bound even if the accurate future power is not known (Fig. 15c)? The answer could be important for scheduling a test (specially, a short duration test) as we may be able to guarantee satisfying thermal constraint

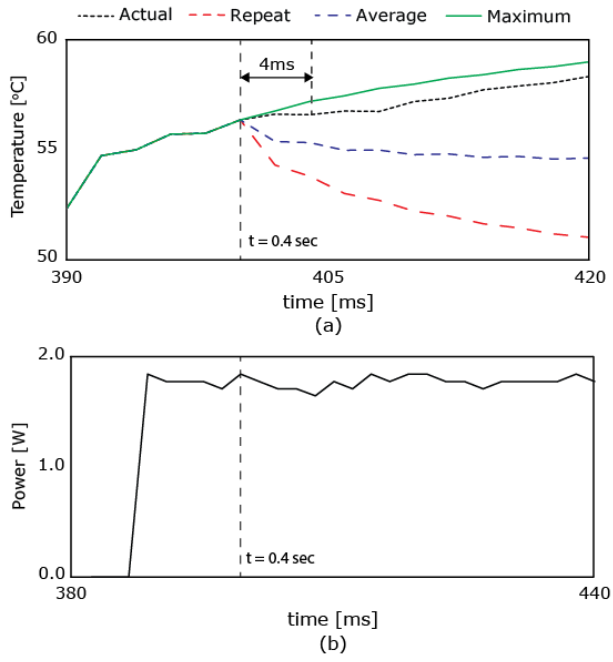

Figure 17. Power prediction if future power is not known: (a) power predicted by three different cases and (b) power pattern near 0.4 second.

over a finite time in future duration without knowing the exact power of that test. The accurate characterization of the thermal property through the filter can provide unique opportunities here. The basis of this study is the fact that due to the phase response as shown in Fig. 8(c), temperature changes slowly with respect to power transition. Hence, at any point of time the temperature variation in the "near" future can have stronger influence of "past" power instead of "current" power. The objective of this study is to estimate the extent of the "near". To perform this study we make three assumptions and study their error characteristics: 1) repeat history of the power pattern, 2) use average power, and 3) use maximum power consumed so far. Here, the power pattern before 0.4 seconds is assumed to be known. This can be obtained by performing the inverse thermal filter (i.e. power estimation) over time (as shown in Fig. 14) which estimates the average power in the past. From the estimated power, we obtain the 1) past power pattern till 0.4 second to be used for repeating, 2) average power of 0.8W up to 0.4 second, and 3) maximum power of 1.9W up to 0.4 second. We observed that the maximum time length for which prediction error is less than 0.5°C is: 1) ~0.2*ms* when repeat pattern is assumed, 2) ~1*ms* when average power is assumed, and 3) ~4*ms* when maximum power is assumed. Fig. 17(a) shows the transient temperature near 0.4 second. Note that maximum power resulted in minimum error partly due to the fact that power peaks near at 0.4 second as shown in Fig. 17(b). Thus, this is not always the case that the assumption of maximum power will result in minimum error. However, considering maximum power may result in most pessimistic assumption and hence, would have a better possibility of guaranteeing the thermal constraint.

VI. Conclusions

In this paper, a test-driven on-line temperature and power estimation approach is proposed utilizing the post-silicon thermal analysis method of Thermal System Identification (TSI). The TSI can be performed during IC testing to uniquely characterize the thermal properties of each IC after fabrication and packaging to consider inherent variations during fabrication. A time-domain forward and inverse thermal filter is designed to estimate temperature (from power) or power (from sensed temperature) in real-time. A mathematical filter is described and the method to optimize the filter parameters is introduced. A test flow is introduced that considers TSI and extracts the time-domain forward and inverse thermal filters to support power-aware and/or thermal-aware testing. Accuracy of proposed time-domain filter is demonstrated with several experiments in a 130nm CMOS test-chip. With the forward thermal filter, temperature was estimated within 3°C error. In addition, average or slowly varying power was effectively estimated within 4% error by using the inverse thermal filter. The proposed time-domain filters provide a unique approach for run-time power and temperature estimations that can enhance the power-aware and thermal-aware testing. Further, the filters define the unique thermal signature of each IC which can be stored in the IC and also used during run-time thermal management. The overall test flow can be repeated

on-line to characterize the time-dependent changes in the thermal filter. The future work on this topic needs to consider hardware implementation of the time-domain filters and explore the potential of on-line real-time power/temperature estimation on power/thermal aware testing.

ACKNOWLEDGMENT

This work is supported by Semiconductor Research Corporation (#2084.001), Intel Corp, and IBM Faculty Award.

REFERENCES

[1] S. Borkar, "Design Challenges of Technology Scaling," in *IEEE Micro*, vol. 19, no.4, pp. 23-29, Jul.-Aug. 1999.

[2] P. Rosinger, B. M. Al-Hashimi, and K. Chakrabarty, "Thermal-Safe Test Scheduling for Core-Based System-On-Chip Integrated Circuits," in *IEEE Tran. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 11, pp. 2502-2512, Nov. 2006.

[3] S. Ravi, "Power-aware Test: Challenges and Solutions," in *IEEE International Test Conference*, pp. 1-10, Oct. 2007.

[4] B. T. Murray and J. P. Hayes, "Testing ICs: Getting to the Core of the Problem," in *IEEE Transactions on Computer*, vol 29, no. 11, pp. 32-38, Nov. 1996.

[5] R. M. Chou, K. K. Saluja, and V. D. Agrawal, "Scheduling Tests for VLSI Systems Under Power Constraints," in *IEEE Tran. on Very Large Scale Integration Systems*, vol. 5, no. 2, pp. 175-185, Jun. 1997.

[6] Z. He, Z. Peng, P. Eles, P. Rosinger, and B. M. Al-Hashimi, "Thermal-Aware SoC Test Scheduling with Test Set Partitioning and Interleaving," in *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems*, pp. 477-485, Oct. 2006.

[7] W. Huang, S. Ghosh, S. Velusamy, K. Sankaranarayanan, K. Skadron, and M. R. Stan, "HotSpot: A Compact Thermal Modeling Methodology for Early-stage VLSI Design," in *IEEE Tran. on Very Large Scale Integration Systems*, vol. 14, no. 5, pp. 501-513, May 2006.

[8] Y. Zhan and S. Sapatnekar, "A High Efficiency Full-Chip Thermal Simulation Algorithm," in *Proc. Int. Conf. on Computer-Aided Design*, pp. 635-638, Nov. 2005.

[9] T. Y. Wang, Y. M. Lee, and C. Chen, "3D Thermal-ADI: An Efficient Chip-level Transient Thermal Simulator," in *Proc. Int. Symp. on Physical Design*, pp. 10-17, Apr. 2003.

[10] T. Yuan, W. Kuo, and S. J. Bae, "Detection of Spatial Defect Patterns Generated in Semiconductor Fabrication Processes," in *IEEE Tran. on Semiconductor Manufacturing*, vol. 24, no. 3, pp. 392-403, Aug. 2011.

[11] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter Variations and Impact on Circuits and Microarchitecture," in *Proc. of Design Automation Conference*, pp.338-342, Jun. 2003.

[12] M. Cho, W. Song, S. Yalamanchili, and S. Mukhopadhyay, "Thermal System Identification (TSI): A Methodology for Post-silicon Characterization and Prediction of the Transient Thermal Field in Multicore Chips," in *IEEE SEMI-THERM Symposium*, pp.118-124, Mar. 2012.

[13] M. Cho, K. Z. Ahmed, W. Song, S. Yalamanchili, and S. Mukhopadhyay, "Methods and Circuits for Post-Silicon Characterization and Prediction of Transient Thermal Field in Integrated Circuits," submitted to *IEEE Tran. on Components, Packaging, and Manufacturing Technologies:* http://www.ece.gatech.edu/research/labs/GREEN /index_files/cho_thermal_system_identification_TCPMT.pdf.

[14] C. Y. Leung, "An Integrated CMOS Current-sensing Circuit for Low-voltage Current-mode Buck Regulator," in *IEEE Tran. Circuits and Systems II*, vol. 52, no. 7, pp. 394-397, Jul. 2005.

[15] N. Mehta, "Dynamic Supply and Threshold Voltage Scaling for CMOS Digital Circuits Using In-Situ Power Monitor," in *IEEE Tran. on Very Large Scale Integration*, vol. 20, no. 5, pp. 892-901, May 2012.

[16] ASTM: Standard Test Method for Thermal Transmission Properties of Thermally Conductive Electrical Insulation Materials, Designation D 5470-12, ASTM International, 2012.

[17] J. Silva-Martinez and S. Solis-Bustos, "Design Considerations for High Performance Very Low Frequency Filters," in *Proc. Int. Symp. on Circuits and Systems*, vol. 2, pp. 648-651, Jun. 1999.

[18] P. Bruschi, G. Barillaro, F. Pieri, and M. Piotto, "Temperature Stabilised Tunable Gm-C Filter for Very Low Frequencies," in *Proc. European Solid-State Circuits Conference*, pp. 107-110, Sep. 2004.

[19] E. Rodriguez-Villegas, A. J. Casson, and Phil Corbishley, "A Subhertz Nanopower Low-Pass Filter," in *IEEE Tran. on Circuits and Systems-II*, vol. 58, no. 6, pp. 351-355, Jun. 2011.

[20] A. G. Radwan, A. M. Soliman, and A. S. Elwakil, "First-oder Filters Generalized to the Fractional Domain," in *Journal of Circuits, Systems, and Computers*, vol. 17, no. 1, pp. 55-66, Feb. 2008.

[21] K. Biswas, S. Sen, and P. K. Dutta, "Realization of a Constant Phase Element and Its Performance Study in a Differentiator Circuit," in *IEEE Tran. on Circuits and Systems-II*, vol. 53, no. 9, pp. 802-806, Sep. 2006.

[22] T. C. Haba, G. Ablart, T. Camps, and F. Olivie, "Influence of the Electrical Parameters on the Input Impedance of a Fractal Structure Realized on Silicon," in *Chaos, Solitons and Fractals*, vol. 24, no. 2, pp. 479-490, Apr. 2005.