A Universal Parallel Front End for Execution Driven Microarchitecture Simulation

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Outline

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- Introduction
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  - Front Ends

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- Those with the resources would prefer not to spend them building incremental prototypes.
- Even if they would, the turn-around time for building a new CPU, even using pre-designed components would be very long.

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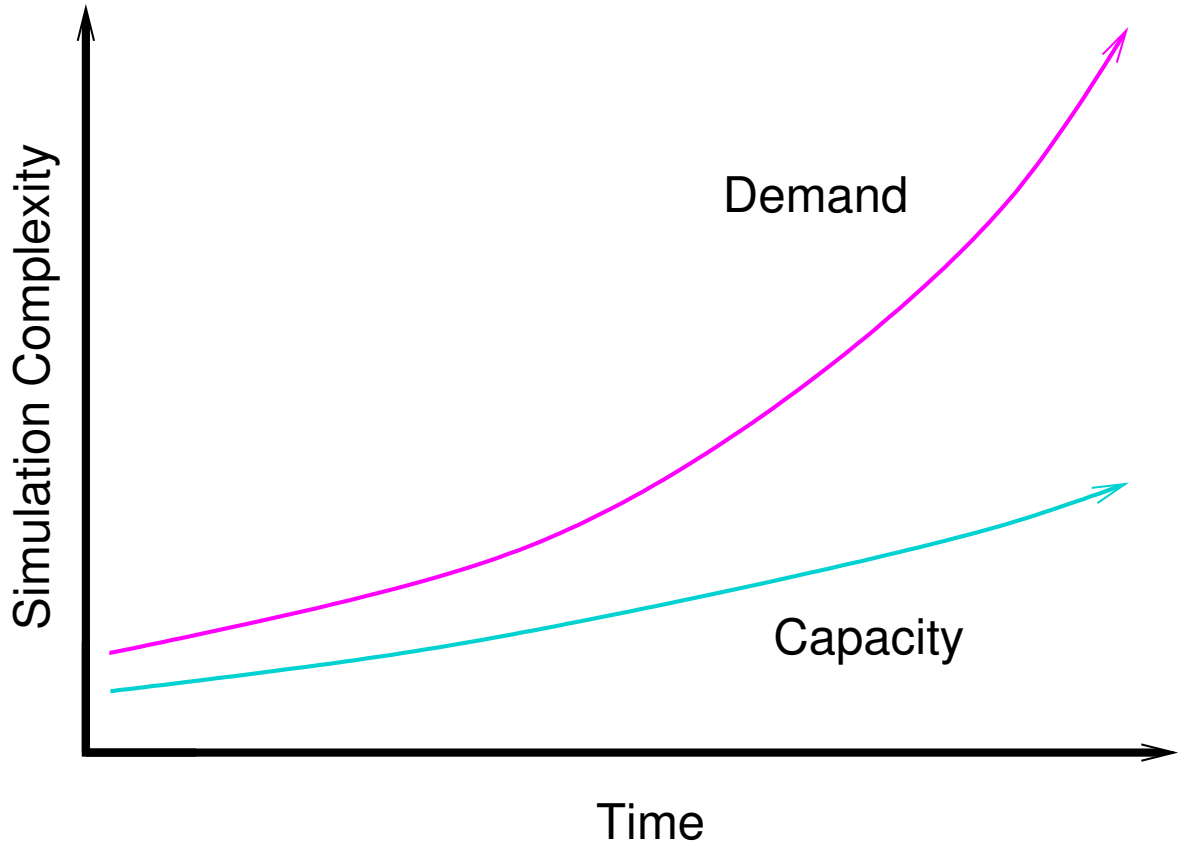

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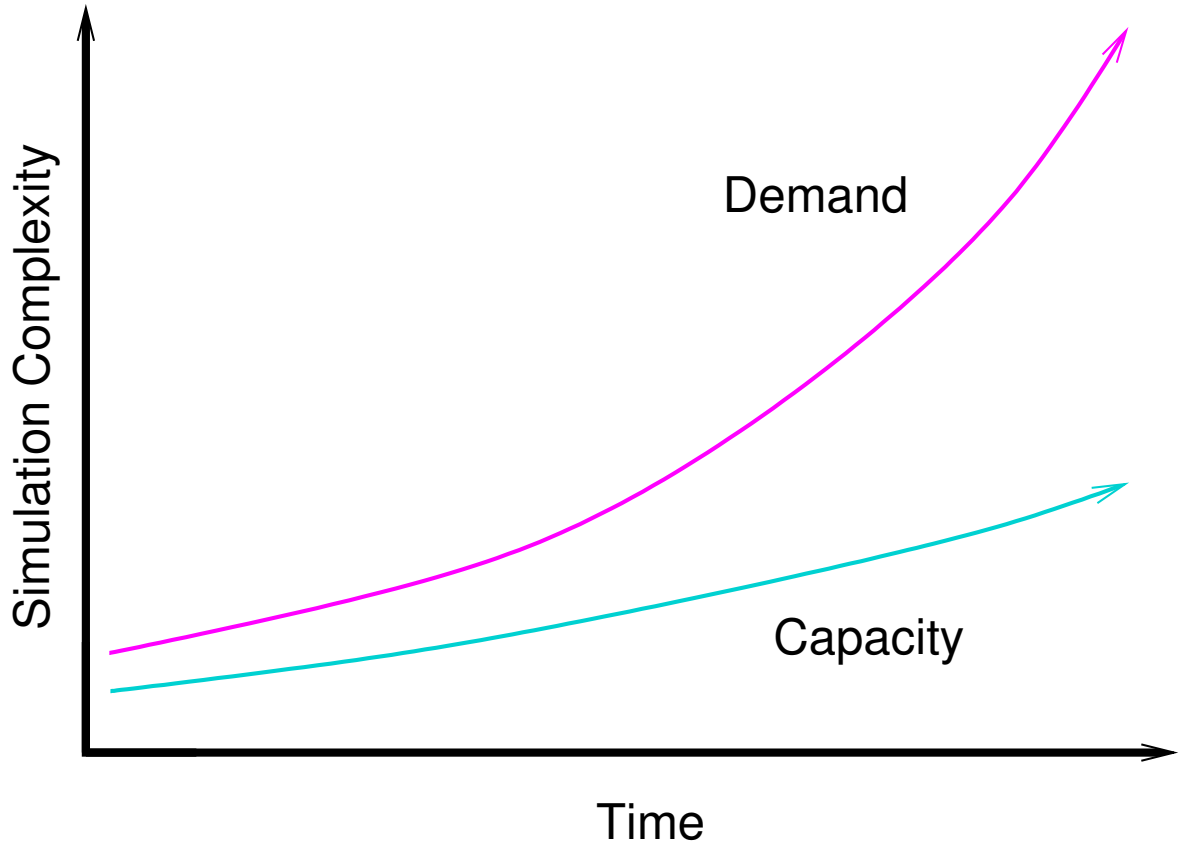

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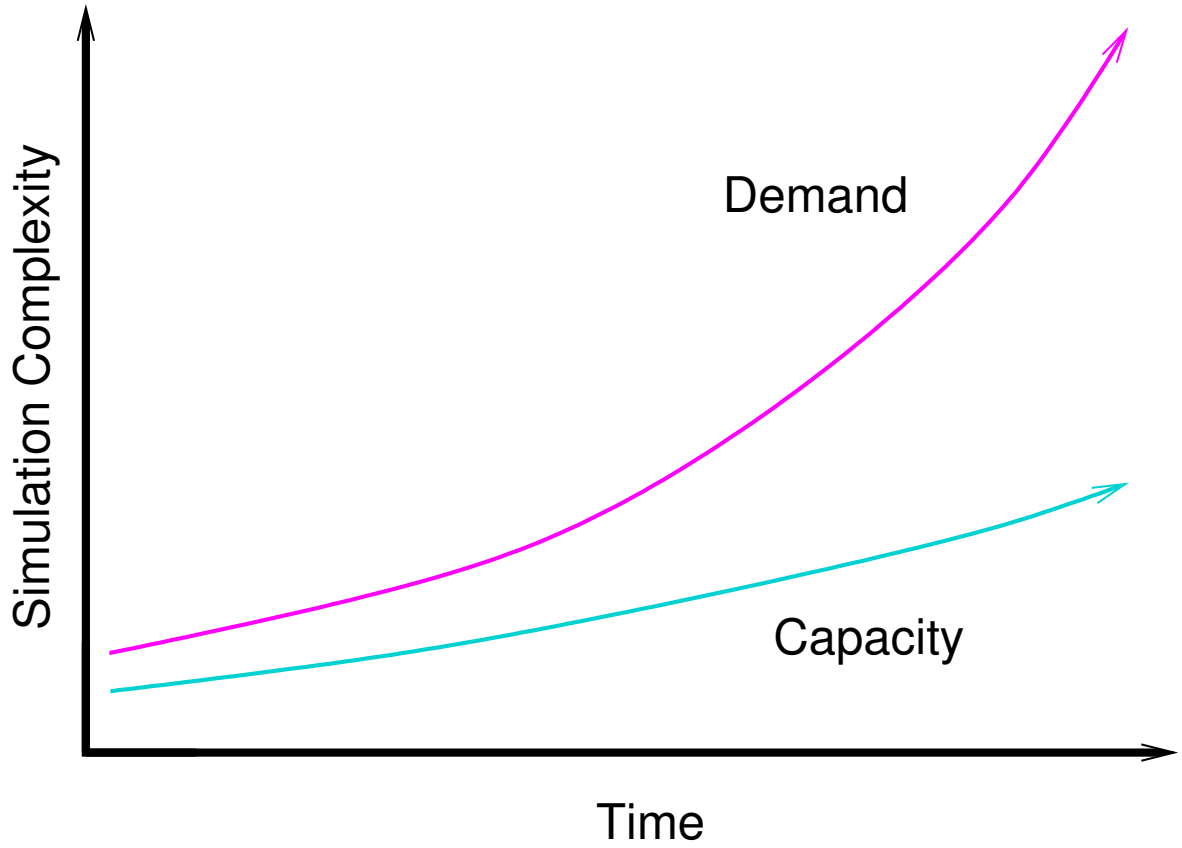

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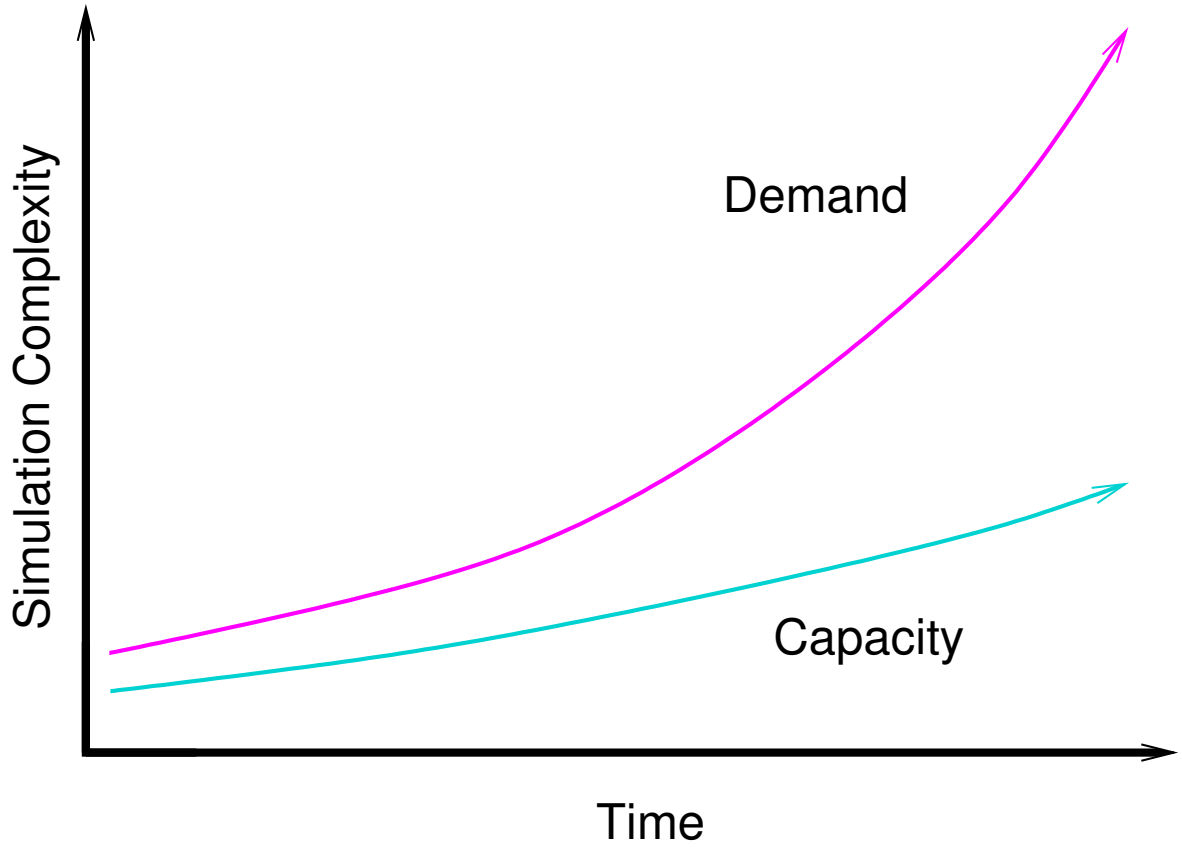

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- Parallel simulation is hard, so we use serial simulators for parallel machines.
- Developments in computer architecture tend to be additive, but we keep building simulators from scratch.

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If we make simulator development more efficient, we increase the rate at which simulation capacity can grow.

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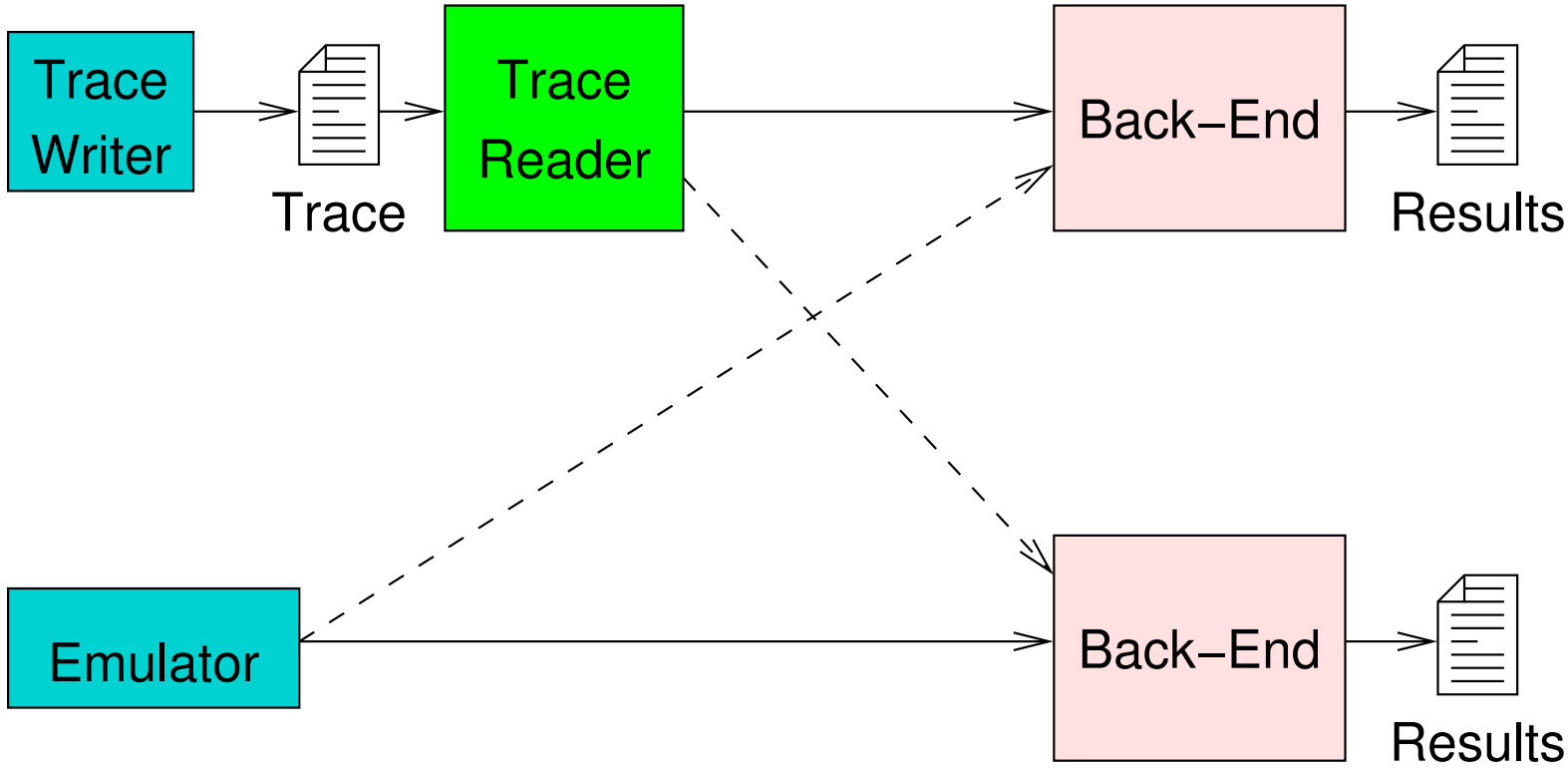
- Back ends are the part that implements the logic that makes a simulator unique.

Introduction– The Ideal Front End



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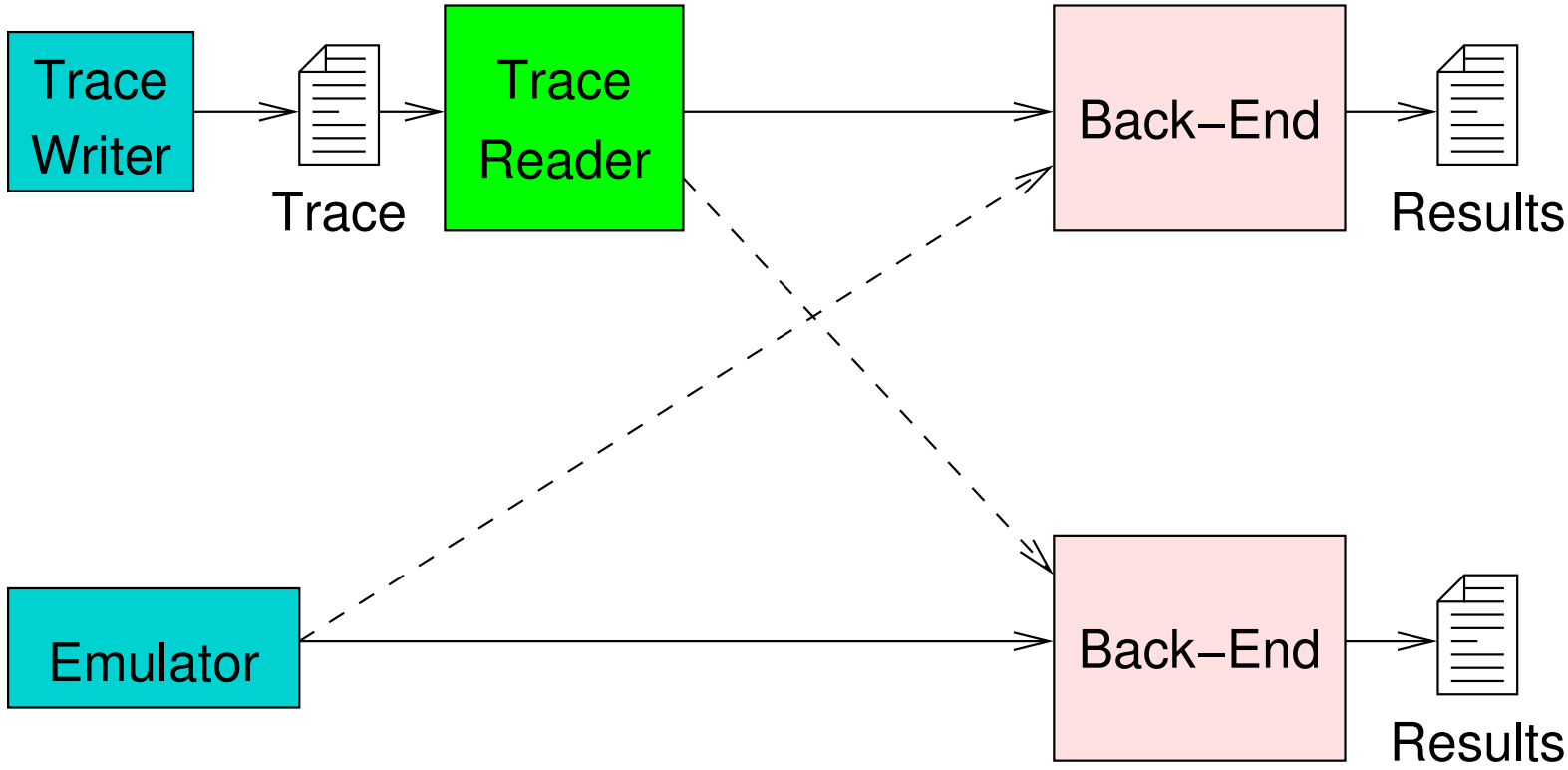

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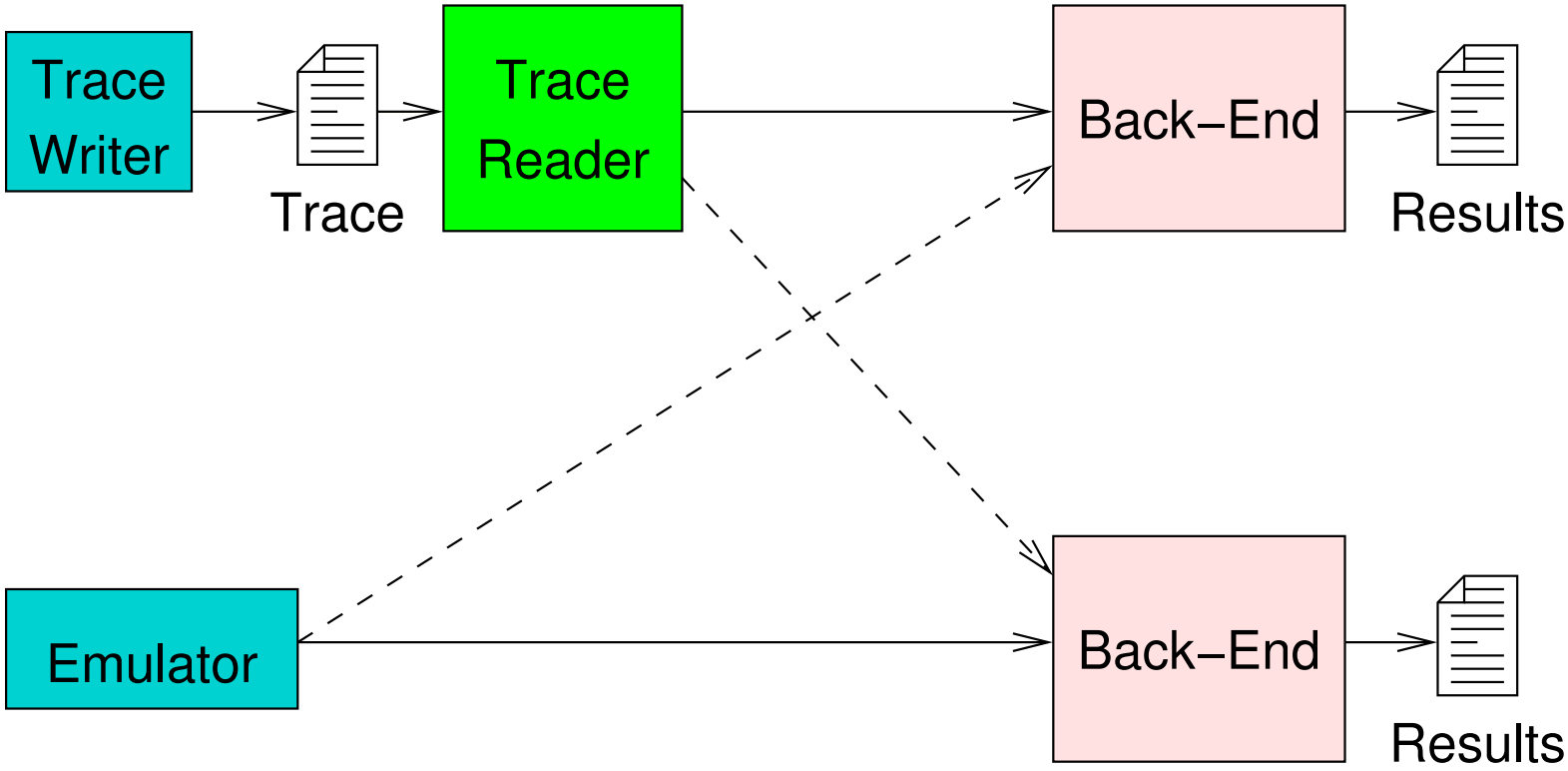

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- Each front end and back end must be written only once, after which they can be used in any combination, like compier front ends and back ends.
- No additional code would need to be written to adapt general purpose emulators for simulation duty.

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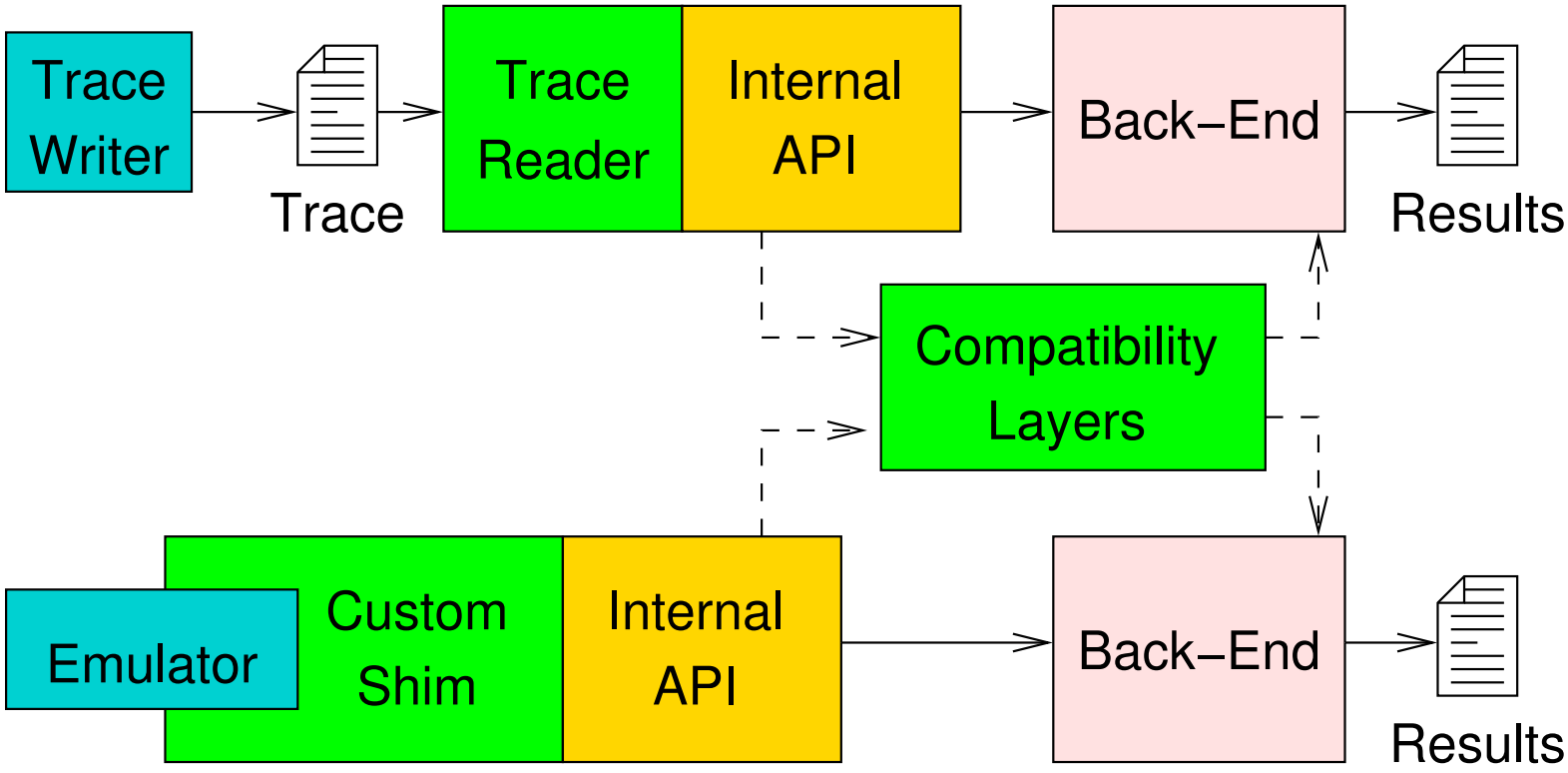

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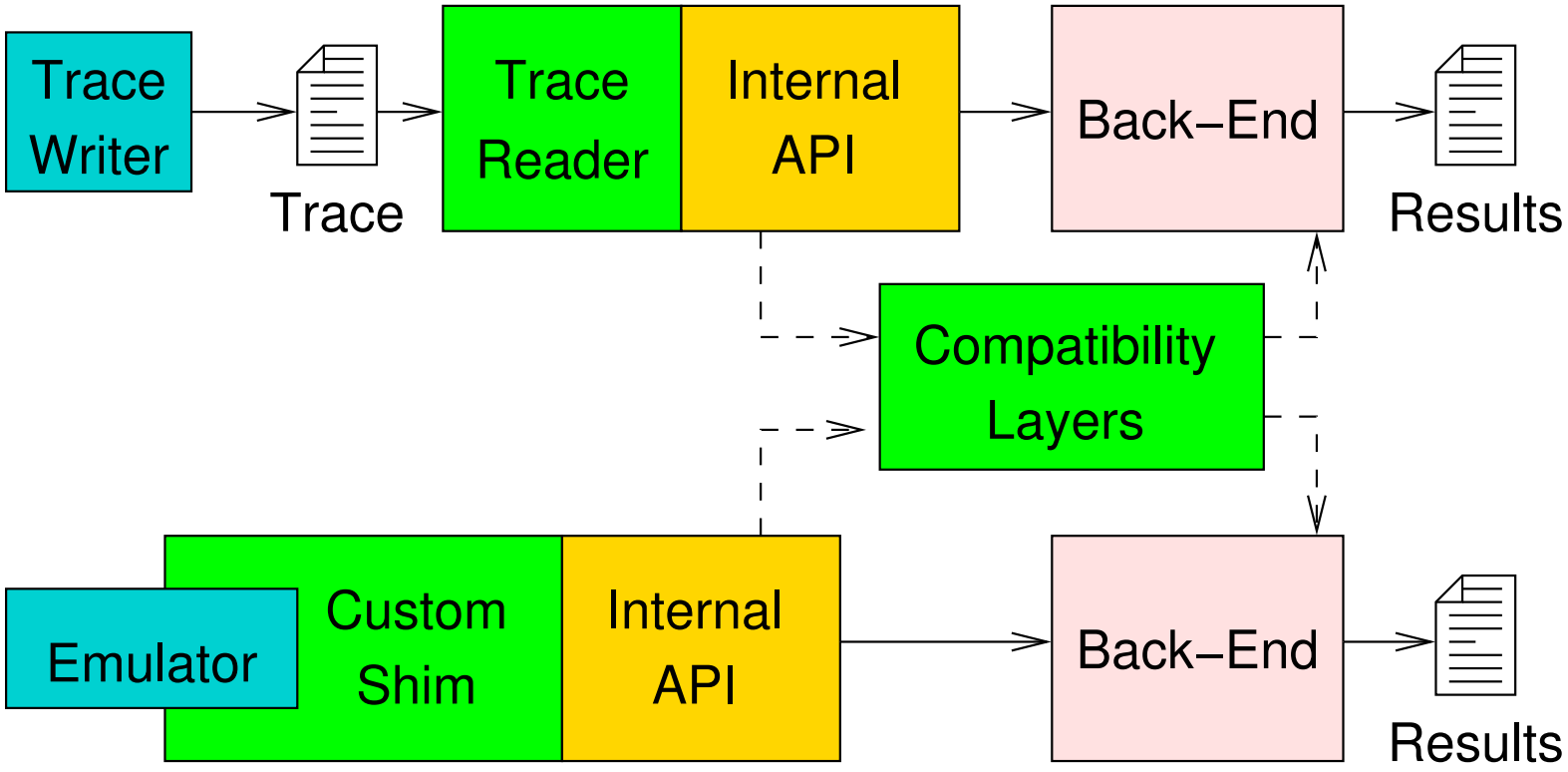

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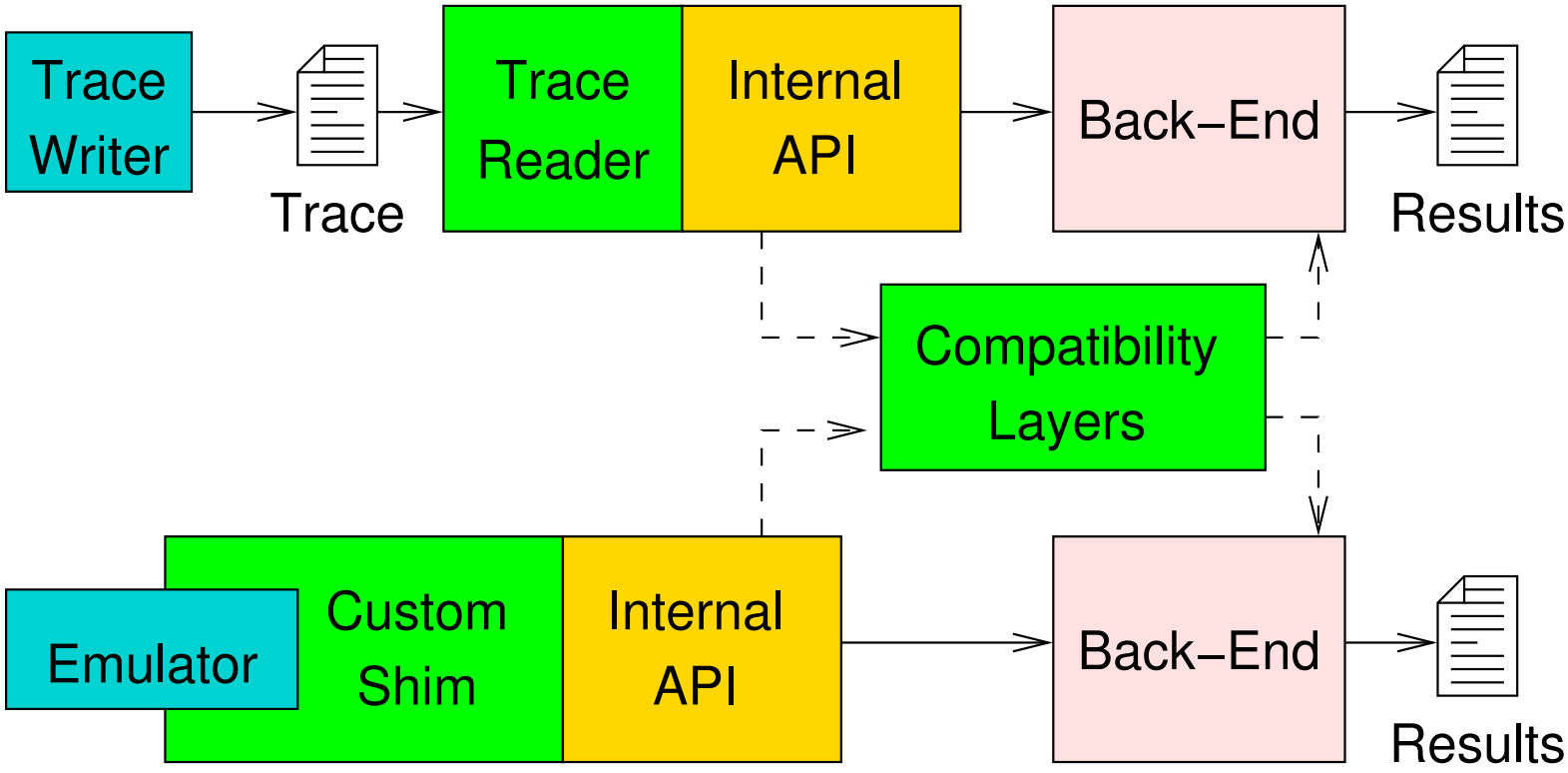

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- Each time this is done, yet another simulator-specific front end is created.

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- Enable the construction of multithreaded simulators.
- Provide sufficient control and detail in the API to make it useable with most back ends.

The QSim Simulator Front End

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  - Enables parallel simulation.

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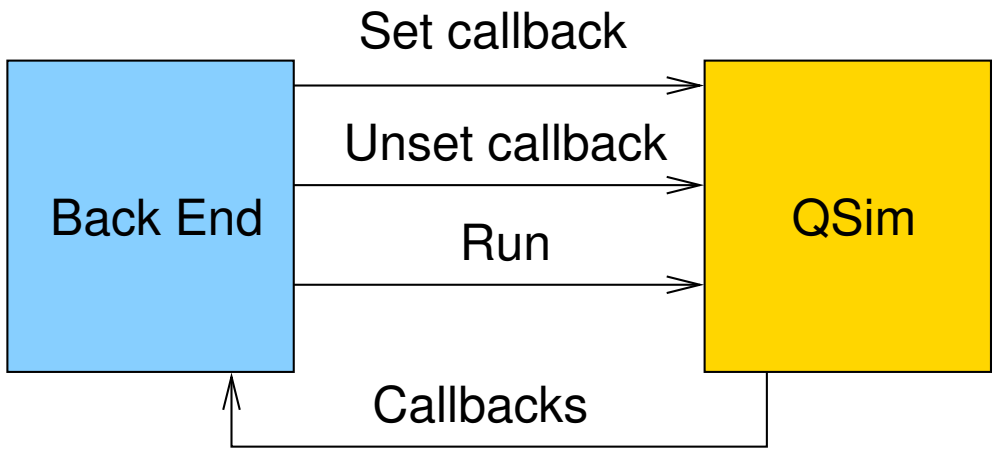
QSim– API Overview



A simplified diagram of the QSim API.

run(i, j)	Advance guest CPU i by j instructions.
set_*_callback(x)	Set callbacks.
unset_*_callback(h)	Unset callbacks by handle.

Callback types include: instruction, register access, memory access, interrupt

QSim– How is it “Universal”?

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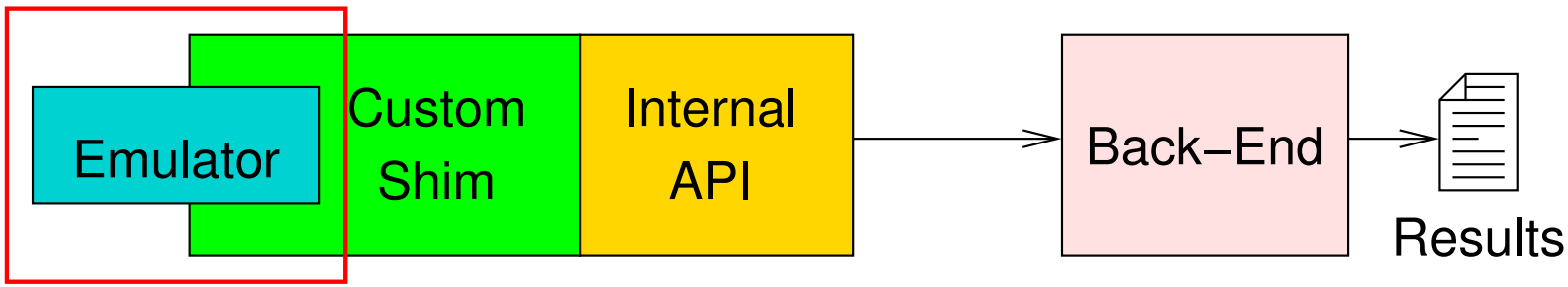

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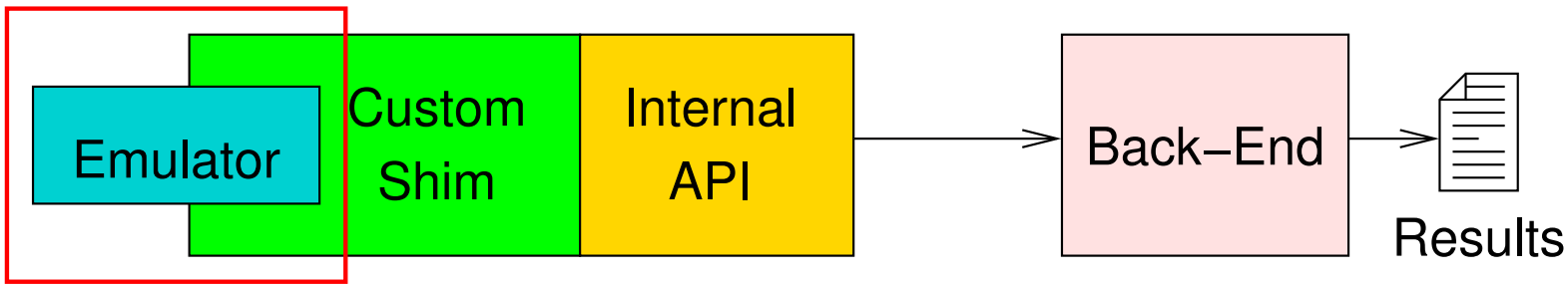

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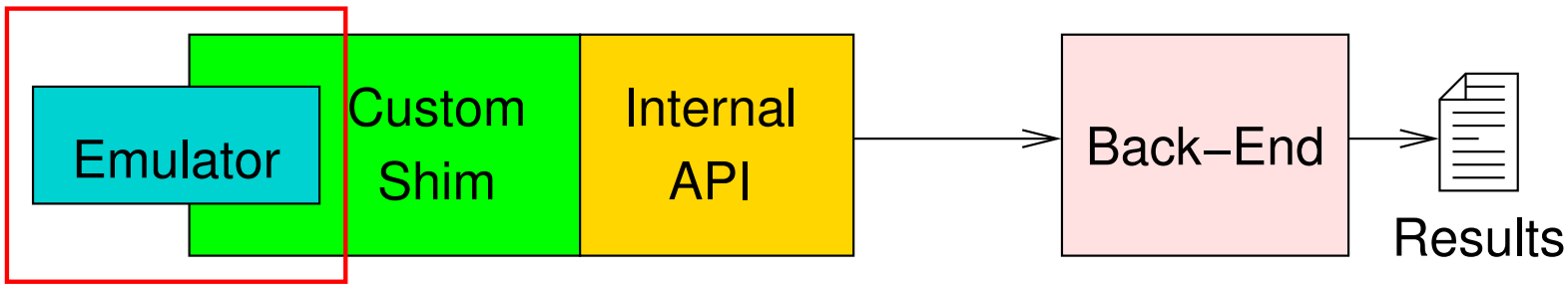

- Off-the-shelf open-source emulators like QEMU provide most of the code needed to build a front end but are incomplete.
- Simulation projects like PTLSim and FAST have modified QEMU heavily to create their front ends.

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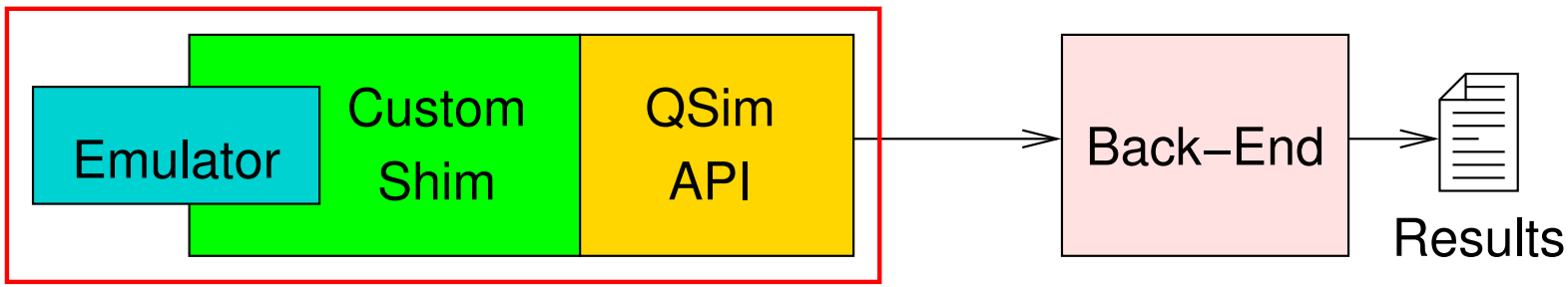

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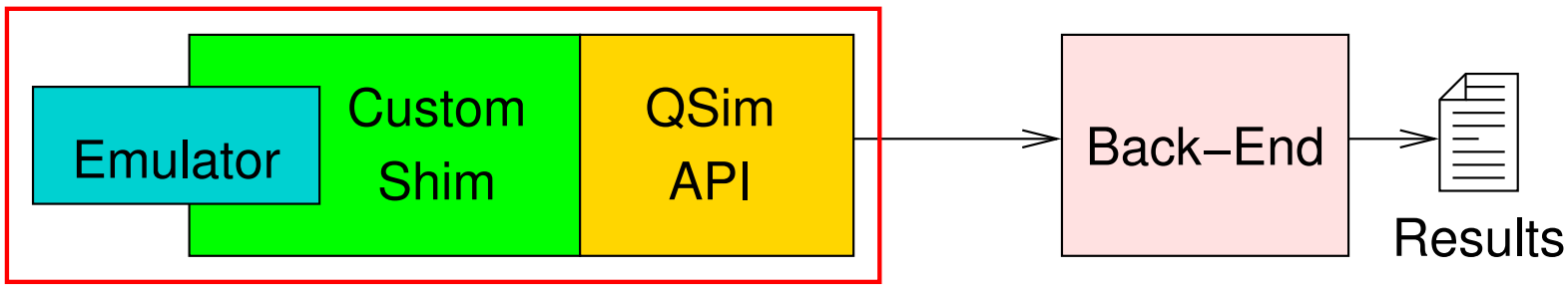

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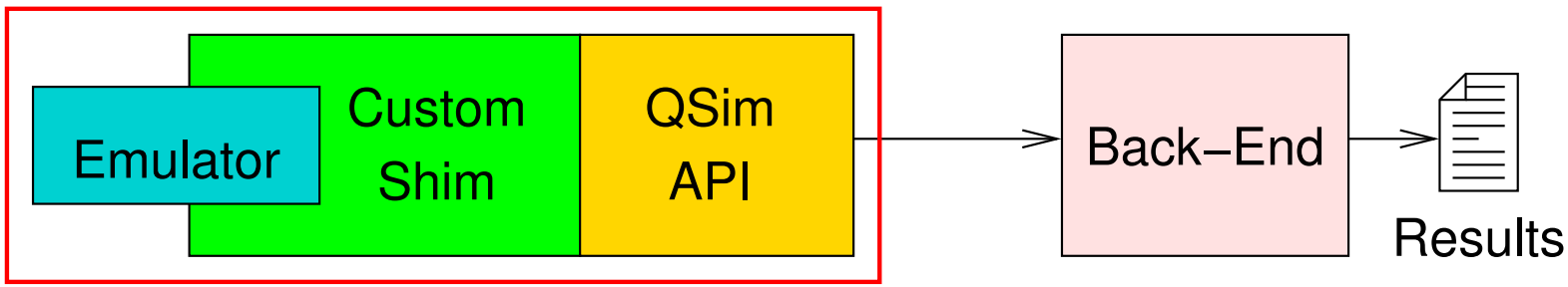

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- Similarly, the API is the same no matter what the instruction set.

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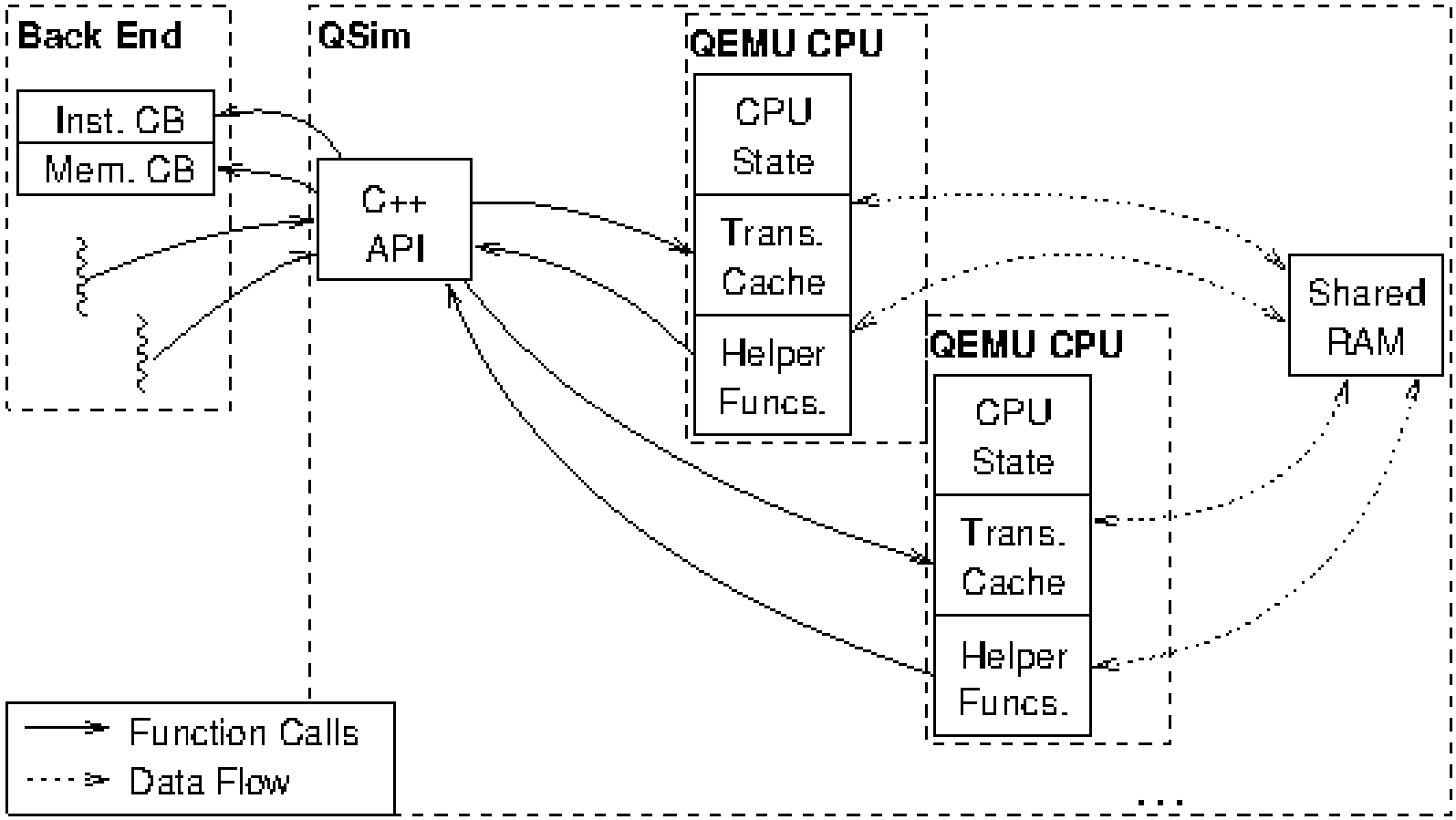
- Up to 512 guest cores have been demonstrated running on up to 512 host threads.

QSim– Software Architecture



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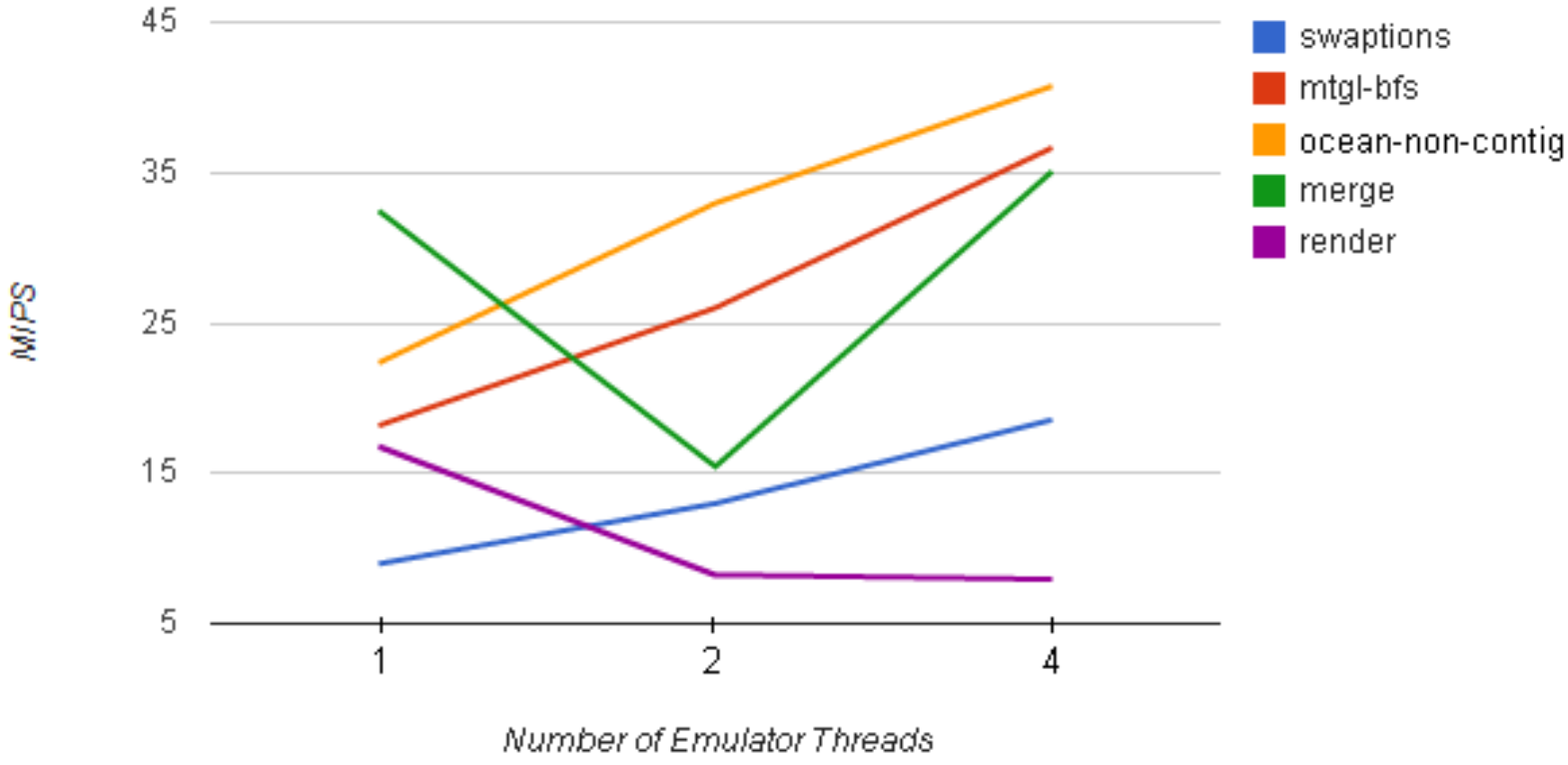

QSim– Performance

The following represents the performance of QSim with empty callbacks. With typical simulation speeds measured in thousands of instructions per second, QSim will not likely be the bottleneck.

Benchmark	**Slowdown**	**MIPS**
swaptions	259x	18.5
mtgl-bfs	387x	36.6
ocean-non-contig	267x	40.7

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Back Ends

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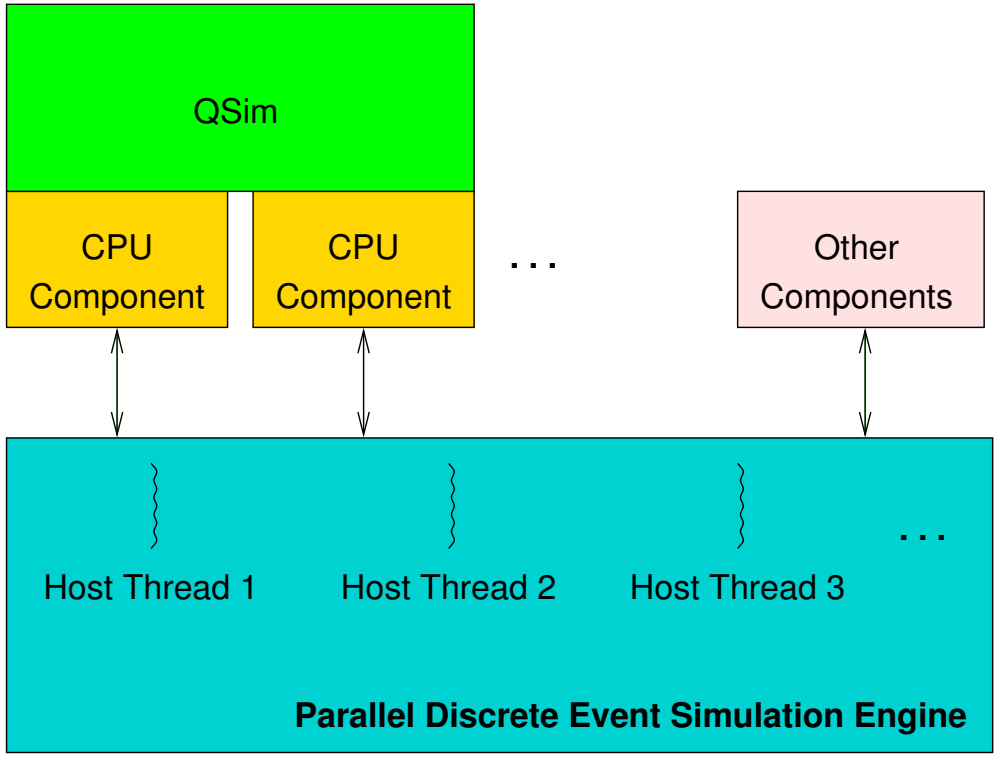

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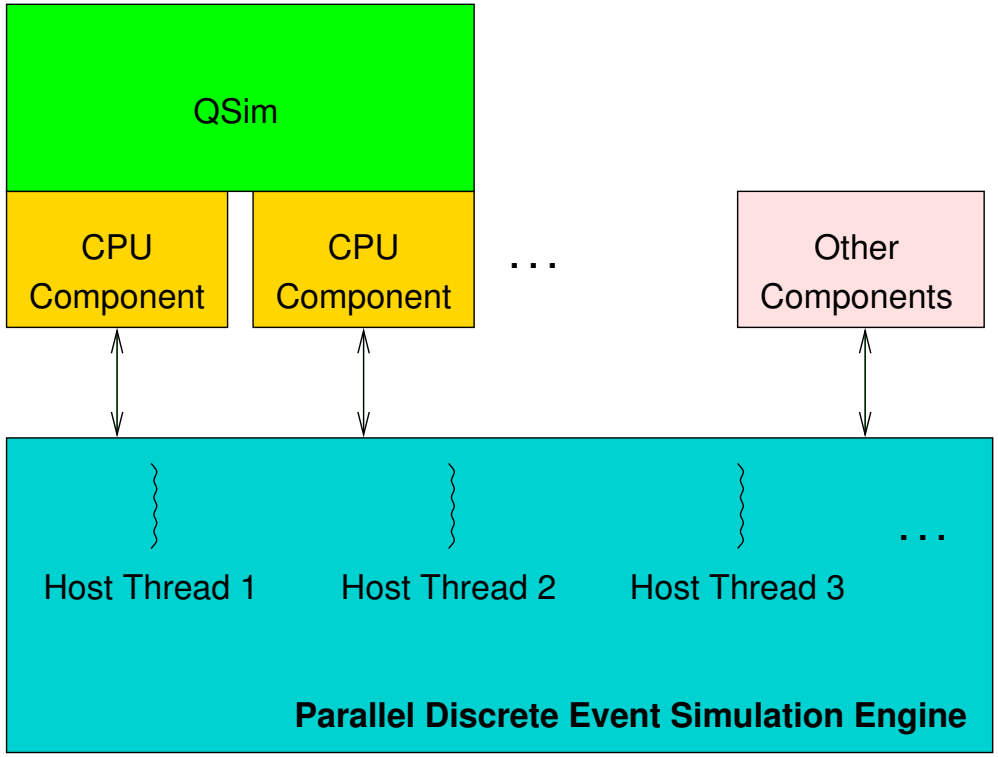

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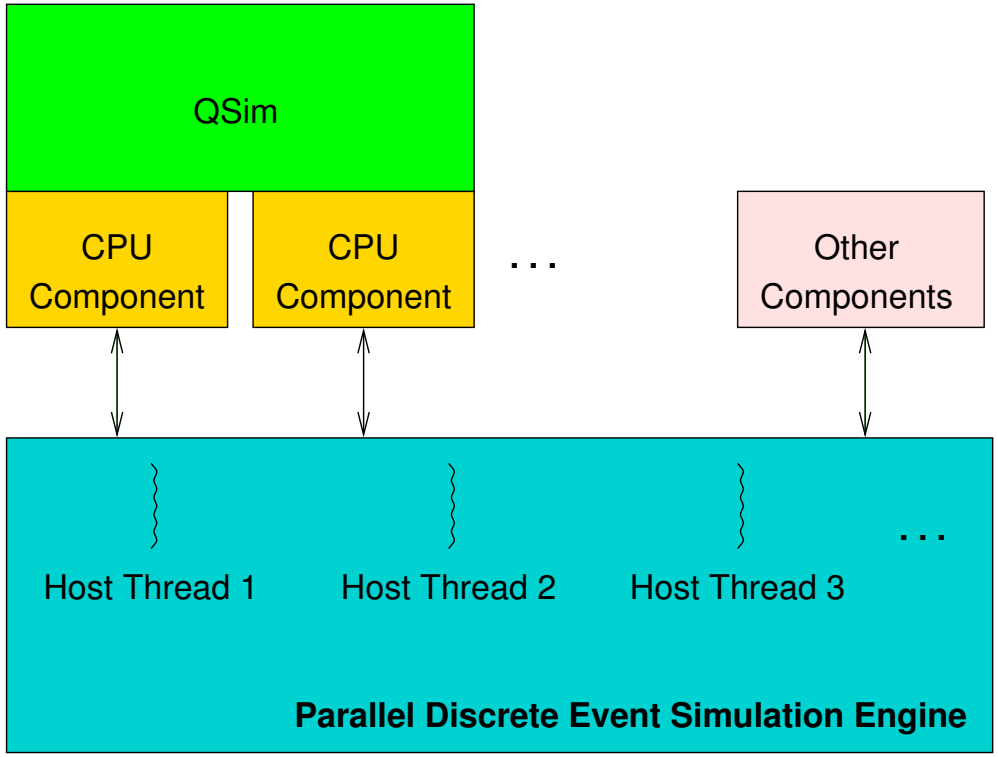

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- A parallel discrete event simulation engine keeps track of events and ensures correctness.

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- Visualization utilities.

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- A plea for parallel front ends.
- A look at how we might narrow the simulation gap.
- An invitation to try QSim[2].

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Acknowledgements

The authors are grateful to Paolo Faraboschi and Daniel Ortega for their suggestions and guidance in getting QSim started. This work was supported by the National Science Foundation under grant CNS855110, Sandia National Laboratories, and HP Laboratories.