A Universal Parallel Front End for Execution Driven Microarchitecture Simulation

Chad D. Kersey
Sudhakar Yalamanchili
Georgia Institute of Technology

Arun Rodrigues
Sandia National Laboratories
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- The QSim Simulator Front End
  - API Overview
  - How is QSim "Universal"?
  - How is it Parallel?
  - How does it Perform?
  - How are QEMU and QSim Related?

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Introduction
Introduction— The Ubiquity of Simulation

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Introduction – The Ubiquity of Simulation

- Simulation is a requirement of architecture research.
- Few architecture researchers have access to the resources needed to create full-scale prototypes.
- Those with the resources would prefer not to spend them building incremental prototypes.
- Even if they would, the turn-around time for building a new CPU, even using pre-designed components would be very long.
Introduction—The Simulation Gap

Reasons for the simulation gap:

▶ Parallel simulation is hard, so we use serial simulators for parallel machines.
▶ Developments in computer architecture tend to be additive, but we keep building simulators from scratch.
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▶ Find ways to make simulator development more efficient.
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- Find ways to make simulator development more efficient.

If we make simulator development more efficient, we increase the rate at which simulation capacity can grow.
Introduction– Front Ends

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▶ Because instruction sets are very complex, front ends are usually created by using and modifying an existing emulation solution or avoiding emulation entirely and tracing native execution.
▶ The back end handles timing, power, and other metrics (how long did that instruction take to clear the pipeline).
▶ Back ends are the part that implements the logic that makes a simulator unique.
Ideally:

Each front end and back end must be written only once, after which they can be used in any combination, like compiler front ends and back ends. No additional code would need to be written to adapt general purpose emulators for simulation duty.
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Introduction— The Ideal Front End

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Introduction – Real Front Ends

Realistically:

- Much custom code needs to be written to adapt most off-the-shelf emulators as simulator front ends.
- Each time this is done, yet another simulator-specific front end is created.
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- Enable the construction of multithreaded simulators.
- Provide sufficient control and detail in the API to make it usable with most back ends.
The QSim Simulator Front End
We have built a simulator front end based on QEMU\(^1\) that aims to address these issues. It currently:

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- Enables the construction of multithreaded simulators.
- Has full support for 32-bit x86 guests. (Port to 64-bit x86 weeks from completion; port to ARM in early coding stages.)

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- Enables the construction of multithreaded simulators.
- Has full support for 32-bit x86 guests. (Port to 64-bit x86 weeks from completion; port to ARM in early coding stages.)
- Enables parallel simulation.

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A simplified diagram of the QSim API.

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td><code>run(i, j)</code></td>
<td>Advance guest CPU $i$ by $j$ instructions.</td>
</tr>
<tr>
<td><code>set_*_callback(x)</code></td>
<td>Set callbacks.</td>
</tr>
<tr>
<td><code>unset_*_callback(h)</code></td>
<td>Unset callbacks by handle.</td>
</tr>
</tbody>
</table>

Callback types include: instruction, register access, memory access, interrupt.
QSim– How is it “Universal”? 

Typical emulator used as a simulator front end:

- Off-the-shelf open-source emulators like QEMU provide most of the code needed to build a front end but are incomplete.
- Simulation projects like PTLSim and FAST have modified QEMU heavily to create their front ends.
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QSim—How is it “Universal”? 

QSim:

- Emulator
- Custom Shim
- QSim API
- Back-End

Results

QSim has done this yet again, but with compatibility with a diverse set of back ends in mind. Similarly, the API is the same no matter what the instruction set.
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The `run()` function can be called simultaneously for two different guest CPUs from different host threads.
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Since back ends tend to use more CPU time than front ends, thread safety is more important than parallel emulation (both are provided by QSim).
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Up to 512 guest cores have been demonstrated running on up to 512 host threads.
QSim– Software Architecture
QSim– Parallel Scaling

The graph shows the parallel scaling of QSim across different emulator thread numbers. The x-axis represents the number of emulator threads, ranging from 1 to 4. The y-axis represents MIPS, ranging from 5 to 45. Different tasks are represented by different colored lines:

- **Blue**: swaptions
- **Red**: mtgl-bfs
- **Orange**: ocean-non-contig
- **Green**: merge
- **Purple**: render

The graph indicates how each task scales with an increasing number of emulator threads.
QSim– Performance

The following represents the performance of QSim with empty callbacks. With typical simulation speeds measured in thousands of instructions per second, QSim will not likely be the bottleneck.

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Slowdown</th>
<th>MIPS</th>
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<tbody>
<tr>
<td>swaptions</td>
<td>259x</td>
<td>18.5</td>
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<td>mtgl-bfs</td>
<td>387x</td>
<td>36.6</td>
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QSim– Relation to QEMU

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- QSim feeds instructions into CPU timing models that are part of a larger simulation infrastructure.
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- A parallel discrete event simulation engine keeps track of events and ensures correctness.
Other back ends that have been built for QSim include:

- A binary trace writer, which was built along with a trace reader library that exports the QSim API.
- A serial universal processor emulator, simplesim.
- A demonstration vehicle; breaks instructions into plausible micro-ops regardless of instruction set.
- An interactive OS/application debugger.
- Visualization utilities.
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▶ An appeal for consistent front end/back end APIs.
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▶ A look at how we might narrow the simulation gap.
▶ An invitation to try QSim².

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The authors are grateful to Paolo Faraboschi and Daniel Ortega for their suggestions and guidance in getting QSim started. This work was supported by the National Science Foundation under grant CNS855110, Sandia National Laboratories, and HP Laboratories.